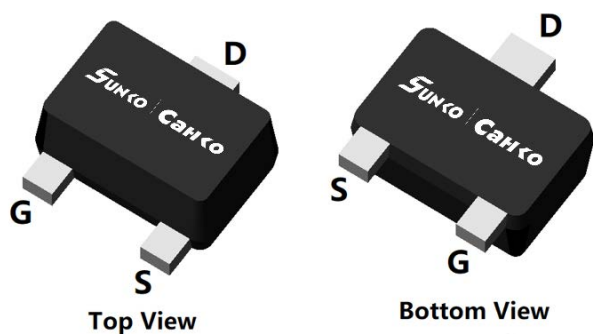
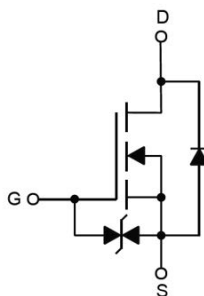


N-Channel Enhancement Mode Field Effect Transistor



SOT-723



Product Summary

- V_{DS} 60V
- I_D 0.3A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.5\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<3\Omega$
- Gate-Source ESD Rating Up to 2KV (HBM)

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	0.3	A
	$T_A=100^\circ\text{C}$		0.2	
Pulsed Drain Current ^A		I_{DM}	0.9	A
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$	P_D	0.34	W
	$T_A=100^\circ\text{C}$		0.13	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^C	Steady-State	$R_{\theta JA}$	300	360	$^\circ\text{C/W}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002KCT	F2	72	8000	80000	320000	7" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
		V _{DS} =60V, V _{GS} =0V, T _j =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.3A	-	1.8	2.5	Ω
		V _{GS} =4.5V, I _D =0.2A	-	2.0	3.0	
Diode Forward Voltage	V _{SD}	I _S =0.3A, V _{GS} =0V	-	0.9	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	130	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	0.3	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz	-	13	-	pF
Output Capacitance	C _{oss}		-	5	-	
Reverse Transfer Capacitance	C _{rss}		-	1	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =0.3A	-	1.22	-	nC
Gate-Source Charge	Q _{gs}		-	0.5	-	
Gate-Drain Charge	Q _{gd}		-	0.18	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.3A, di/dt=100A/us	-	3.6	-	nC
Reverse Recovery Time	t _{rr}		-	16	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =0.3A R _{GEN} =50Ω	-	7	-	ns
Turn-on Rise Time	t _r		-	19	-	
Turn-off Delay Time	t _{D(off)}		-	20	-	
Turn-off fall Time	t _f		-	84	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

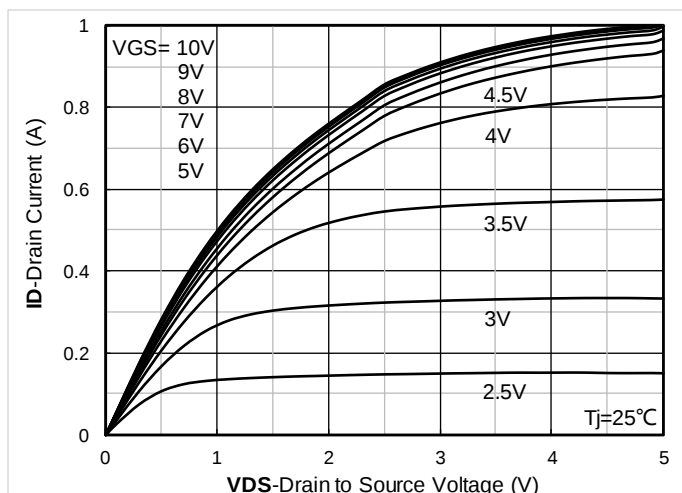


Figure 1. Output Characteristics

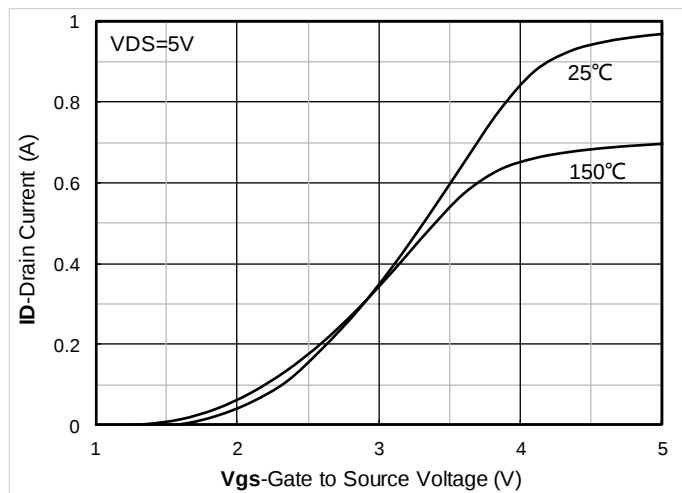


Figure 2. Transfer Characteristics

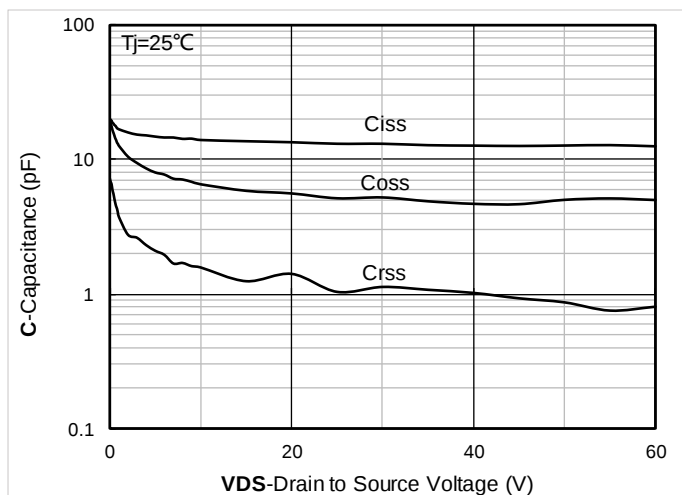


Figure 3. Capacitance Characteristics

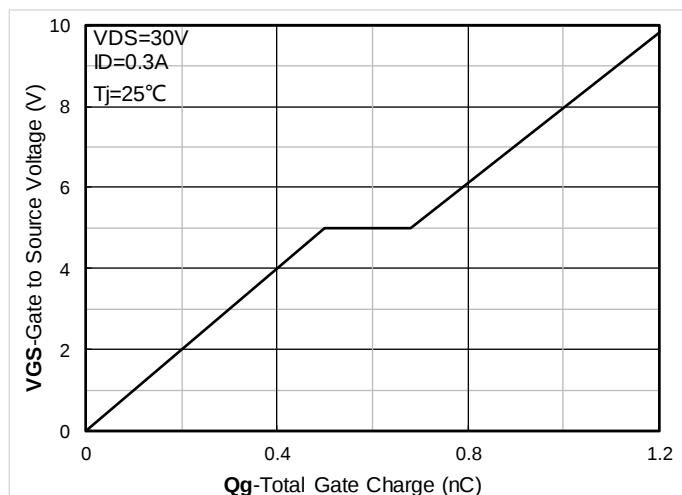


Figure 4. Gate Charge

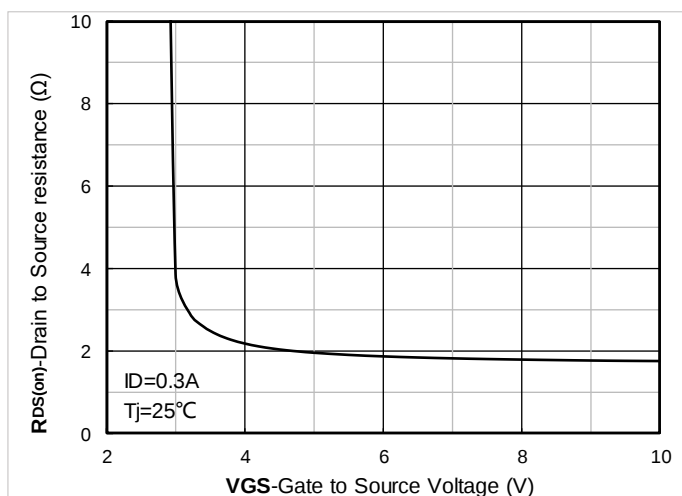


Figure 5. On-Resistance vs Gate to Source Voltage

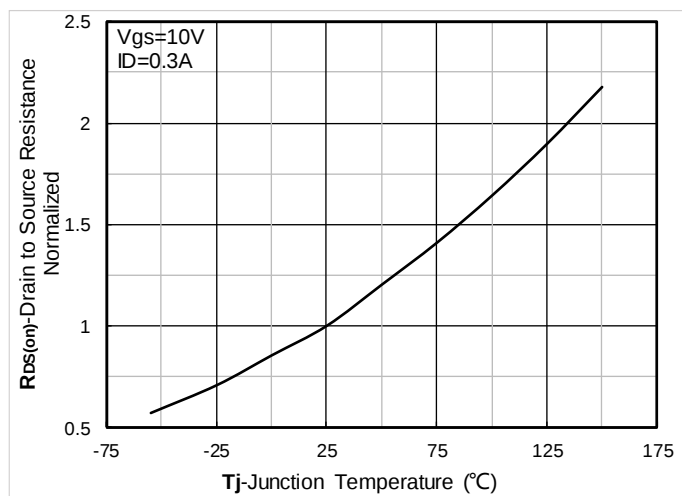


Figure 6. Normalized On-Resistance

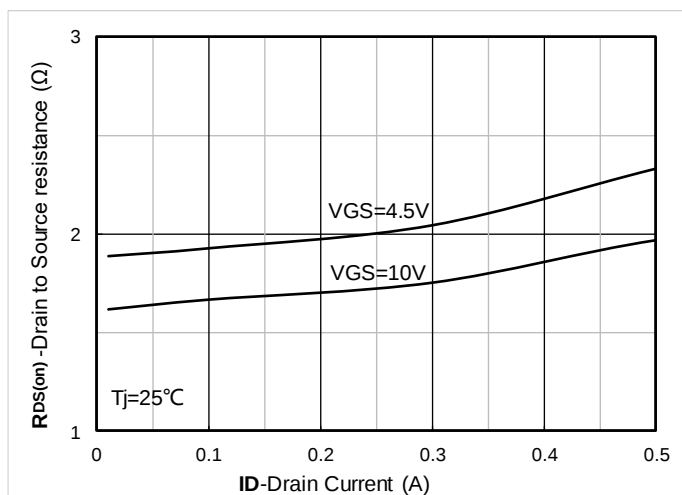


Figure 7. RDS(on) VS Drain Current

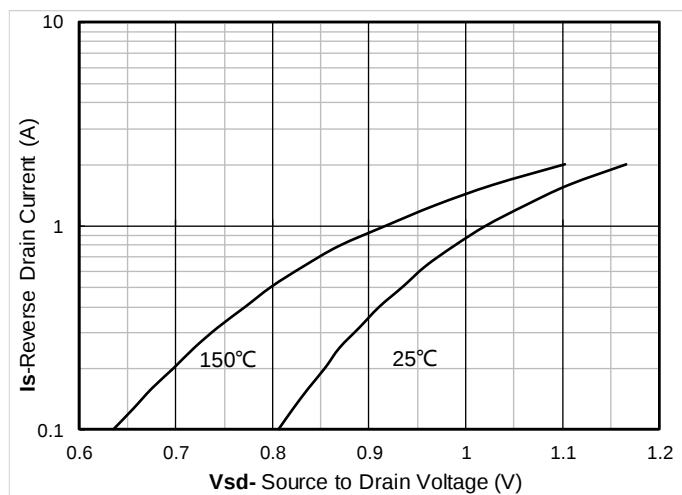


Figure 8. Forward characteristics of reverse diode

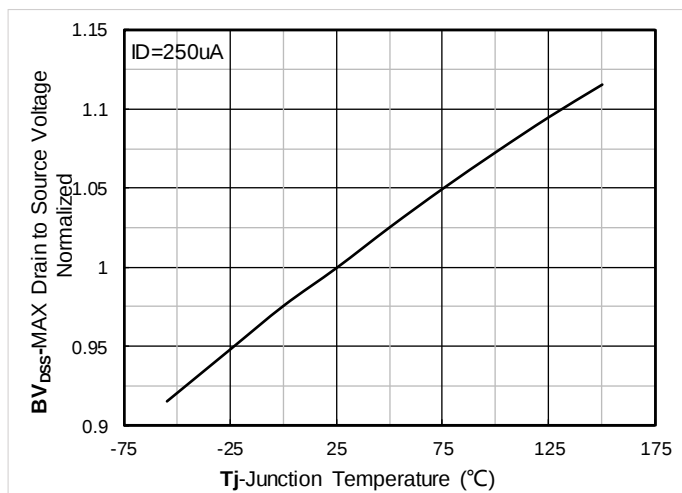


Figure 9 Standardized breakdown voltage

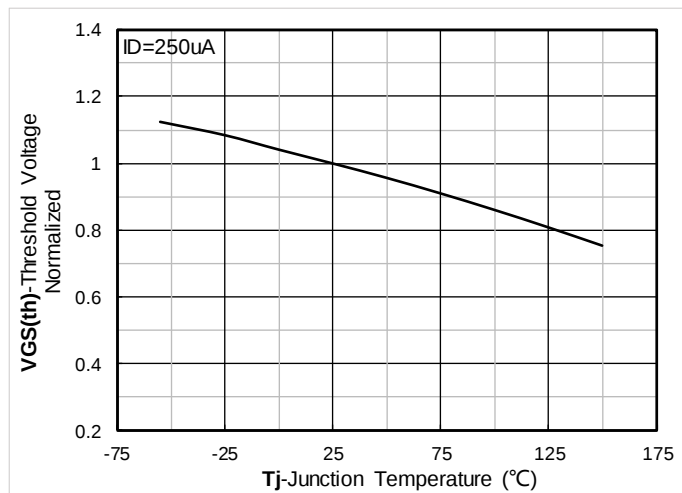


Figure 10. normalized threshold voltage

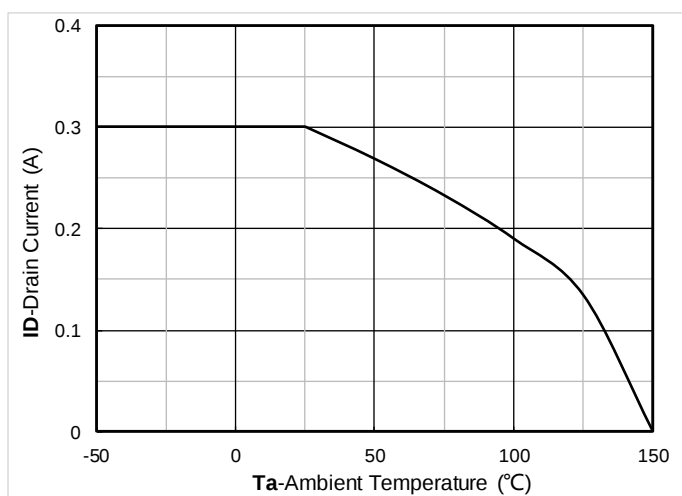


Figure 11 Current dissipation

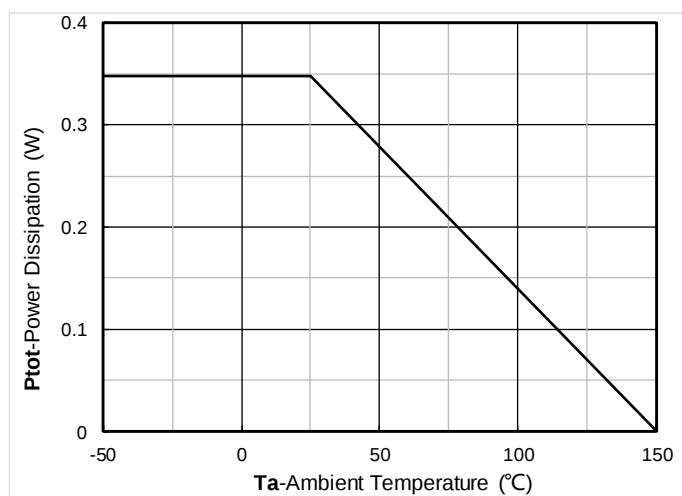


Figure 12 Power scattering

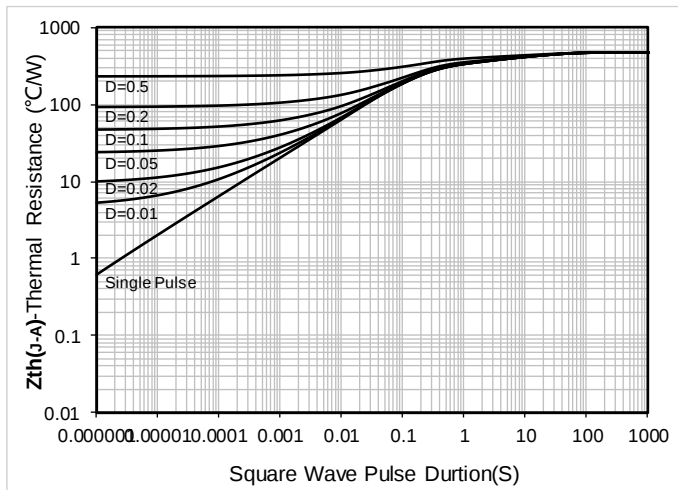


Figure 13 Maximum transition resistance

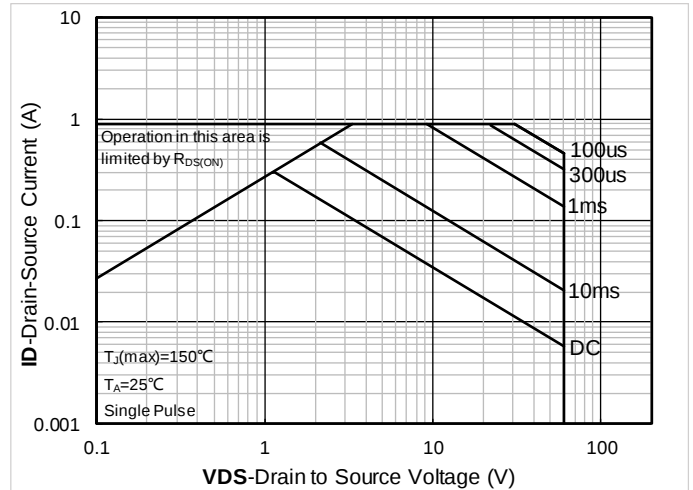


Figure 14 Safe working area

■ Test circuit and waveform

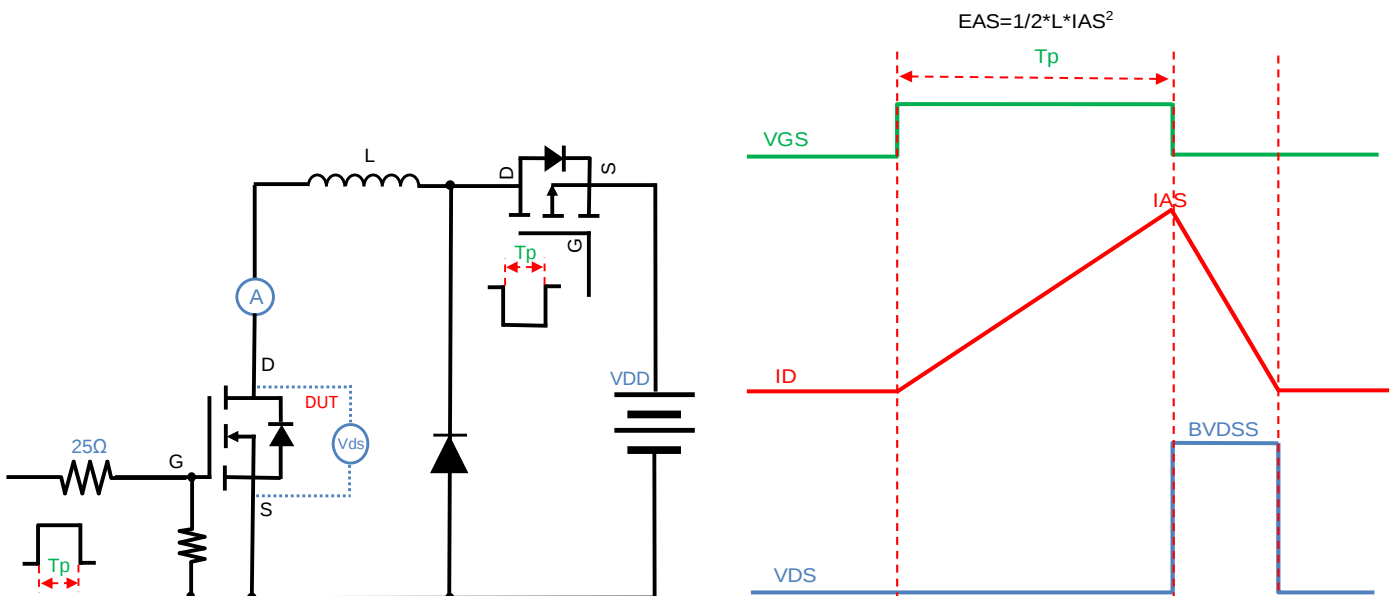


Figure A. Test circuit and waveform of unlit induction switch (UIS)



Figure B. Grid Charge Test Circuit and Waveform

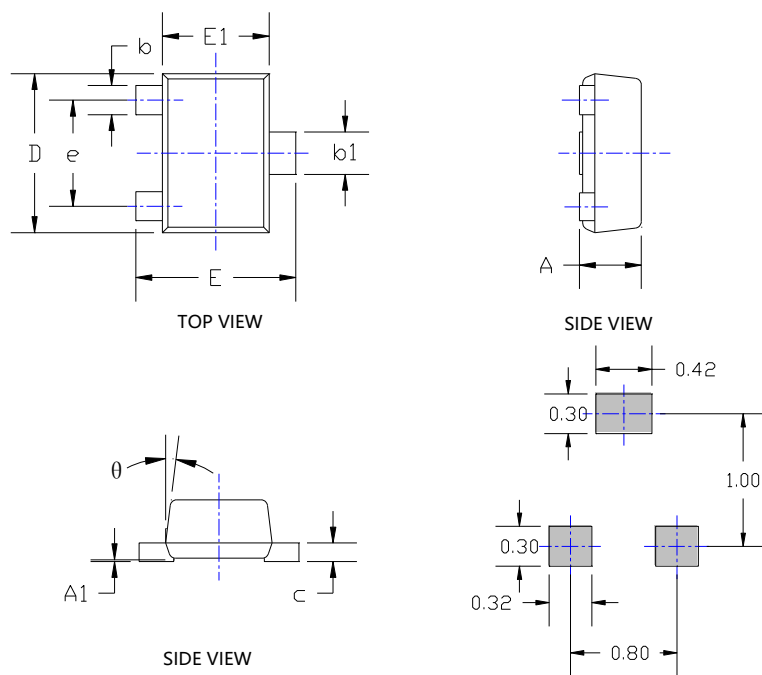


Figure C. Resistance switch test circuit and waveform



Figure D. Diode Recovery Test Circuit and Waveform

■ Packaging Information SOT-723



Suggested disk layout

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031 TYP.		0.800 TYP.	
θ	7° REF.		7° REF.	

Note:

1. The packaging size does not include mold burrs and sprue burrs.

2. Acceptance, unless otherwise specified,

It is 0.1 millimeters.

3. The position of the welding plate is for reference only.

To Disclaimer phenomenon

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