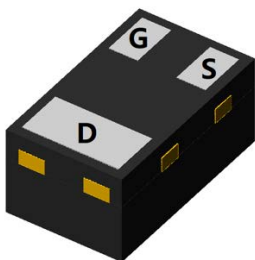


P-Channel Enhancement Mode Field Effect Transistor

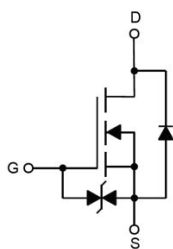


Top View



Bottom View

DFN1006-3L



Product Summary

- V_{DS} -20V
- I_D -0.65A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <850 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <1200 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-1.8V$) <2000 mohm
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Interfacing, Logic switch
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 12	V
Drain Current	$T_A=25^{\circ}C$ Steady State	I_D	-0.65	A
	$T_A=70^{\circ}C$ Steady State		-0.52	
Pulsed Drain Current ^A		I_{DM}	-2.0	A
Total Power Dissipation @ $T_A=25^{\circ}C$ Steady State		P_D	0.9	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	138	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCA3139KB	F1	9A	10000	100000	400000	7" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V		±1.5	±10	μA
		V _{GS} = ±8V, V _{DS} =0V		±500	±2000	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D =-0.5A		580	850	mΩ
		V _{GS} = -2.5V, I _D =-0.3A		855	1200	
		V _{GS} = -1.8V, I _D =-0.2A		1350	2000	
Diode Forward Voltage	V _{SD}	I _S =-0.65A, V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-0.65	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		71		pF
Output Capacitance	C _{oss}			20		
Reverse Transfer Capacitance	C _{rss}			15		
Gate resistance	R _g	f=1MHz, Open Drain		85		Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DD} =-10V, I _D =-0.5A		1.24		nC
Gate Source Charge	Q _{gs}			0.37		
Gate Drain Charge	Q _{gd}			0.27		
Reverse Recovery Chrage	Q _{rr}	I _F =-0.5A, di/dt=-20A/us		0.97		ns
Reverse Recovery Time	t _{rr}			26		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DD} =-10V, R _L =2.5Ω, R _{GEN} =3Ω		4		
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			16		
Turn-off Fall Time	t _f			25		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_D is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

■ Typical Performance Characteristics

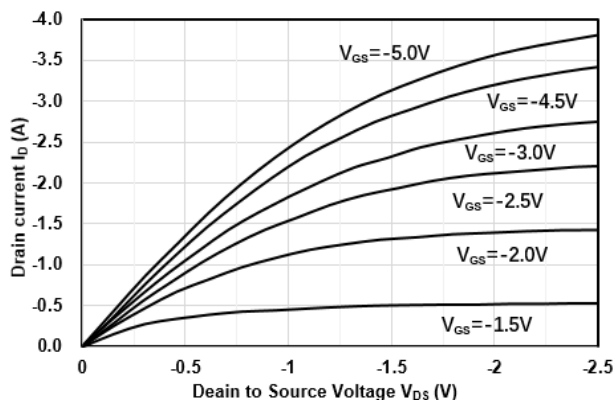


Figure1. Output Characteristics

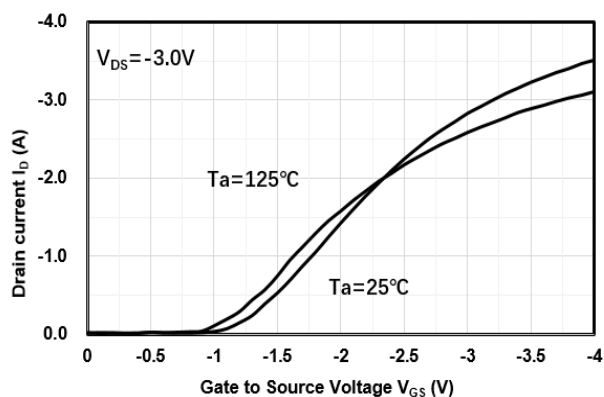


Figure2. Transfer Characteristics

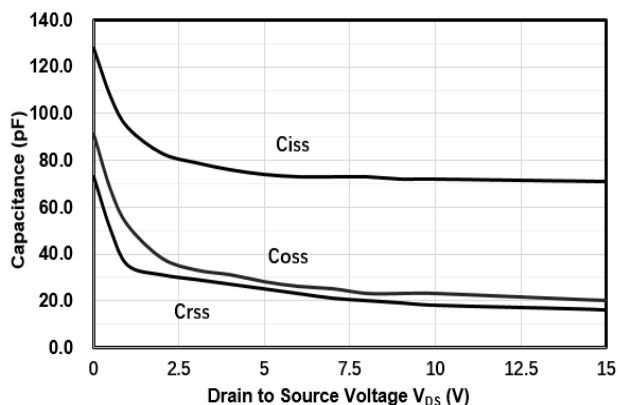


Figure3. Capacitance Characteristics

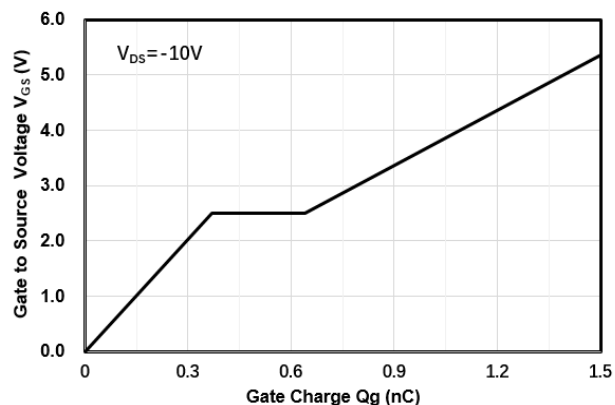


Figure4. Gate Charge

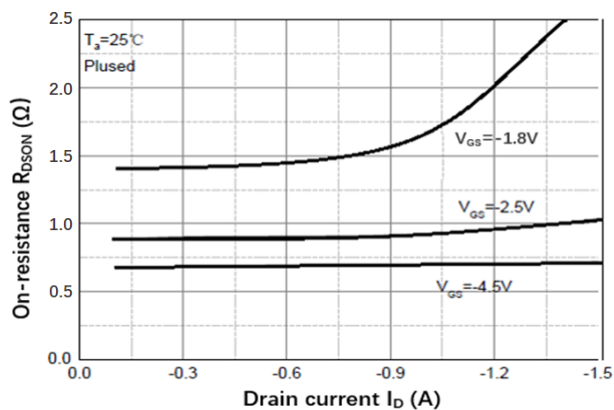


Figure5. Drain-Source on Resistance

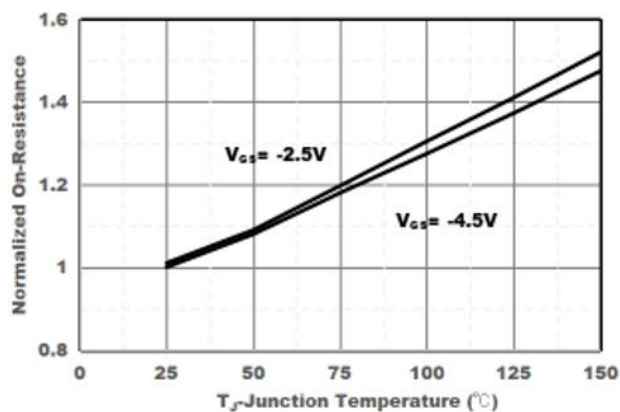


Figure6. Drain-Source on Resistance

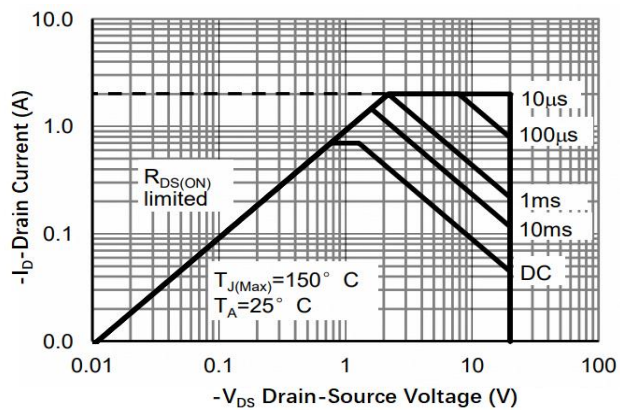


Figure7. Safe Operation Area

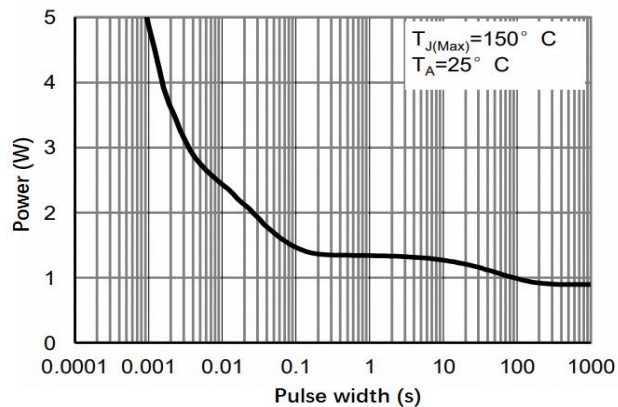


Figure8. Pulse Power Rating Junction-to Ambient

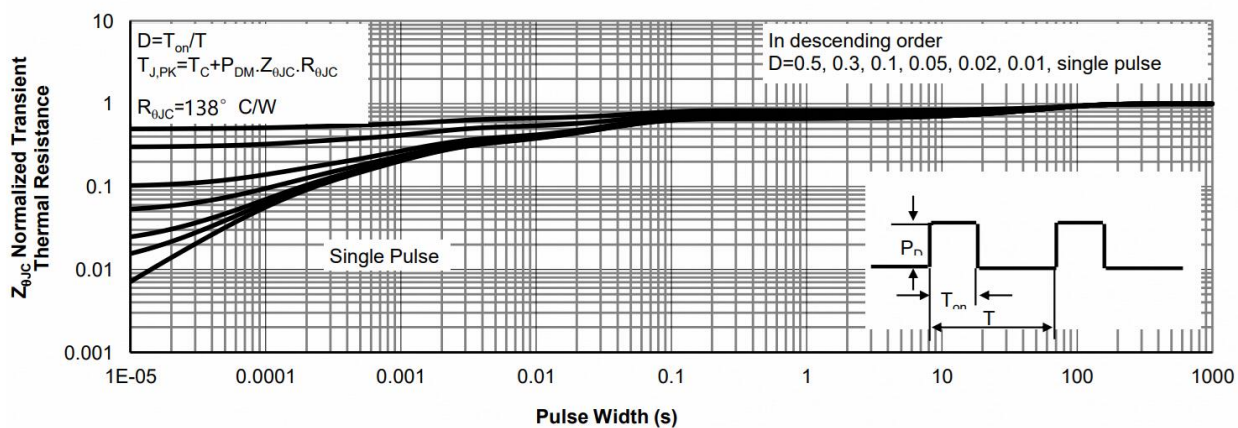
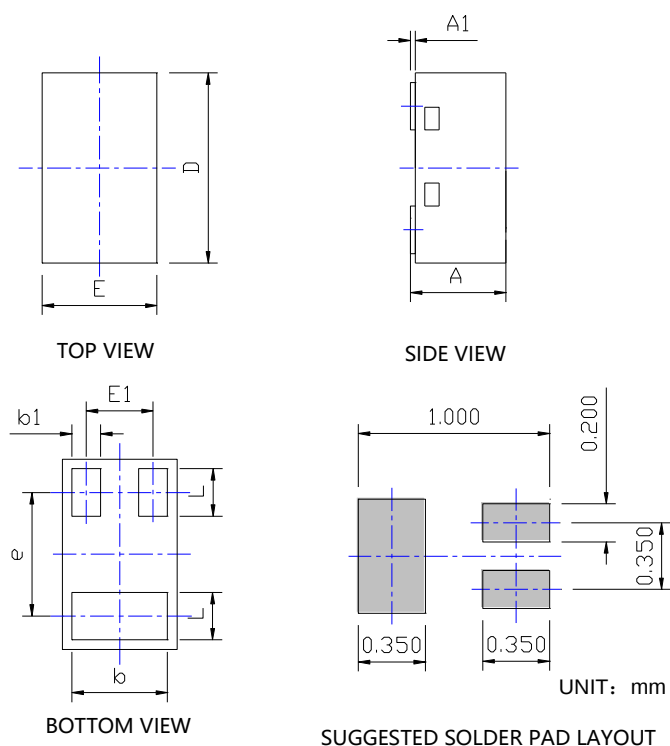


Figure9. Normalized Maximum Transient Thermal Impedance

■ DFN1006-3L Package information



SYMBOL	DIMENSIONS		
	Millimeter		
	MIN.	NOM.	MAX.
A	0.42	---	0.55
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L	0.20	0.25	0.30

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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