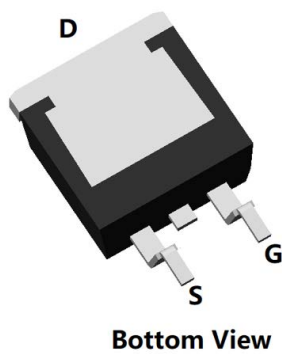
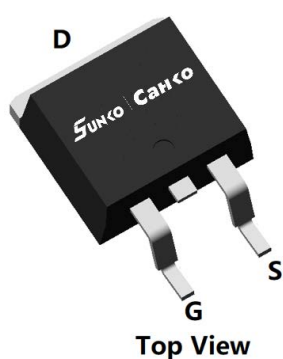
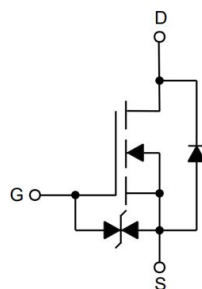


N-Channel Enhancement Mode Field Effect Transistor



TO-263



Product Summary

• V_{DS}	100V
• I_D	130A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<5.5mohm
• $R_{DS(ON)}$ (at $V_{GS}=6V$)	<6.5mohm
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	15	A
	$T_A=100^\circ\text{C}$		9	
	$T_C=25^\circ\text{C}$		130	
	$T_C=100^\circ\text{C}$		82	
Pulsed Drain Current ^A		I_{DM}	520	A
Avalanche energy ^B		EAS	290	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	2.7	W
	$T_A=100^\circ\text{C}$		1.1	
	$T_C=25^\circ\text{C}$		178	
	$T_C=100^\circ\text{C}$		71	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	35	45	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.55	0.7	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCB130G10B	F2 SC	B130G10B	800	/	8000	13" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	2.8	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =65A	-	4	5.5	mΩ
		V _{GS} =10V, I _D =20A	-	4	5.5	
		V _{GS} =6V, I _D =20A	-	5	6.5	
Diode Forward Voltage	V _{SD}	I _S =65A, V _{GS} =0V	-	0.9	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	0.8	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	130	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	4300	-	pF
Output Capacitance	C _{oss}		-	2000	-	
Reverse Transfer Capacitance	C _{rss}		-	25	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =65A	-	60	-	nC
Gate-Source Charge	Q _{gs}		-	17	-	
Gate-Drain Charge	Q _{gd}		-	19	-	
Reverse Recovery Charge	Q _{rr}	I _F =65A, di/dt=600A/us	-	170	-	nC
Reverse Recovery Time	t _{rr}		-	40	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =65A R _{GEN} =2.2Ω	-	20	-	ns
Turn-on Rise Time	t _r		-	100	-	
Turn-off Delay Time	t _{D(off)}		-	30	-	
Turn-off fall Time	t _f		-	8	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=50V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=34A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

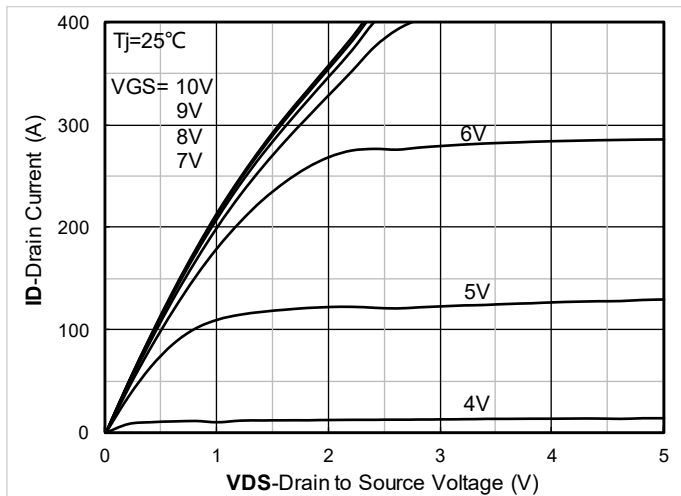


Figure1. Output Characteristics

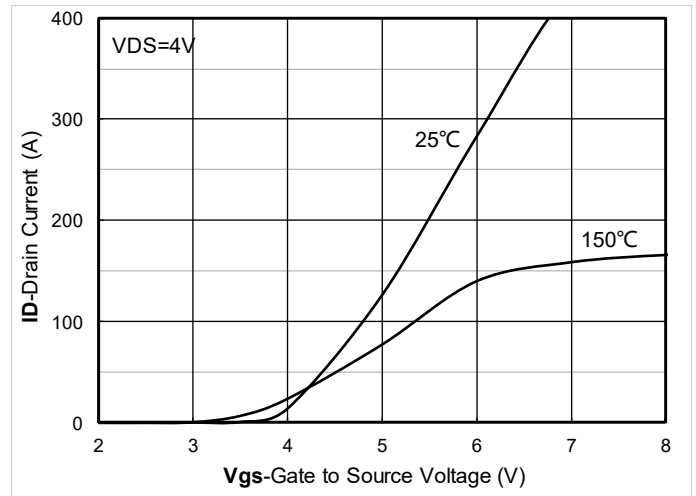


Figure2. Transfer Characteristics

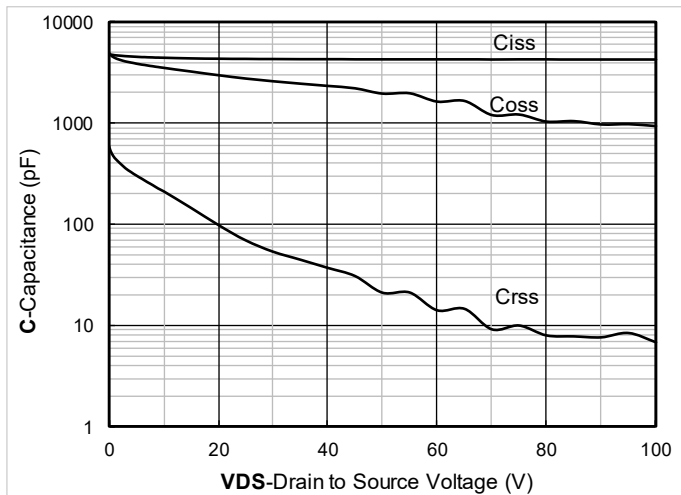


Figure3. Capacitance Characteristics

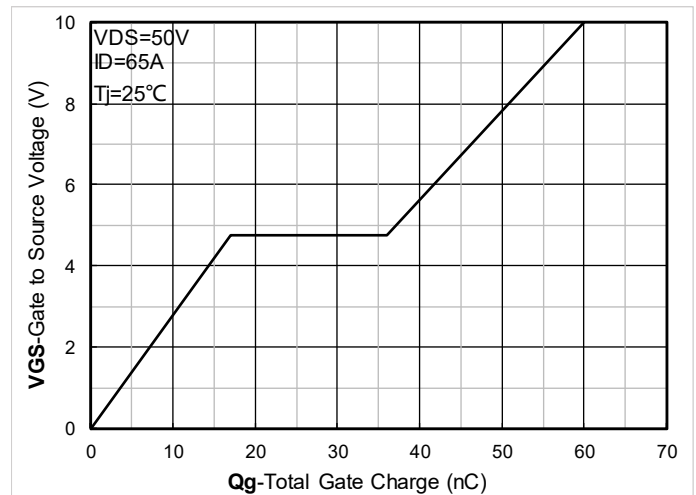


Figure4. Gate Charge

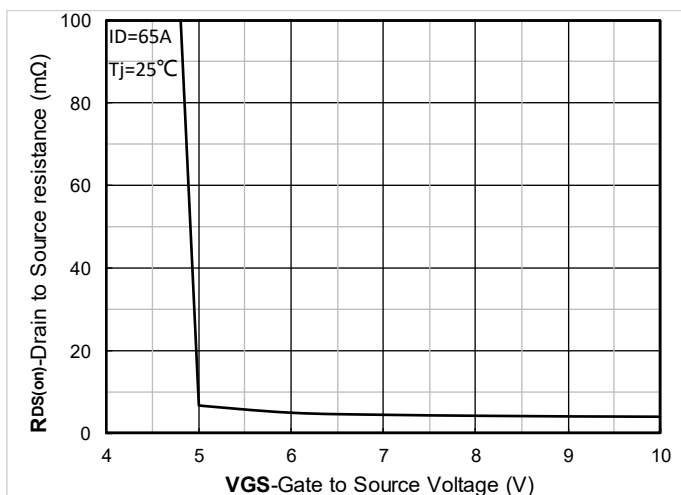


Figure5. On-Resistance vs Gate to Source Voltage

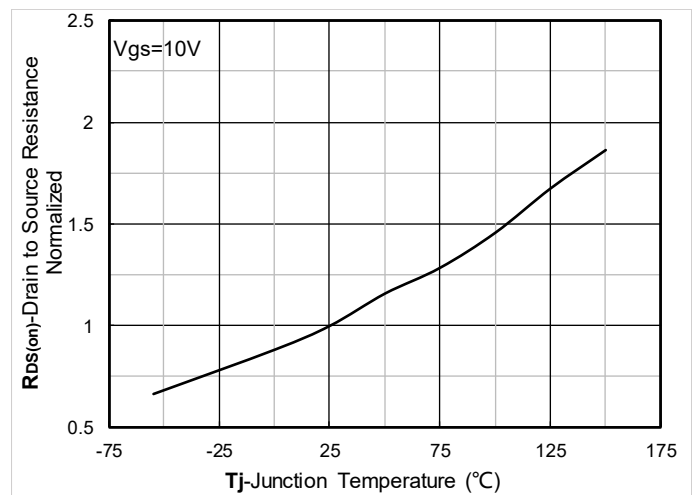


Figure6. Normalized On-Resistance

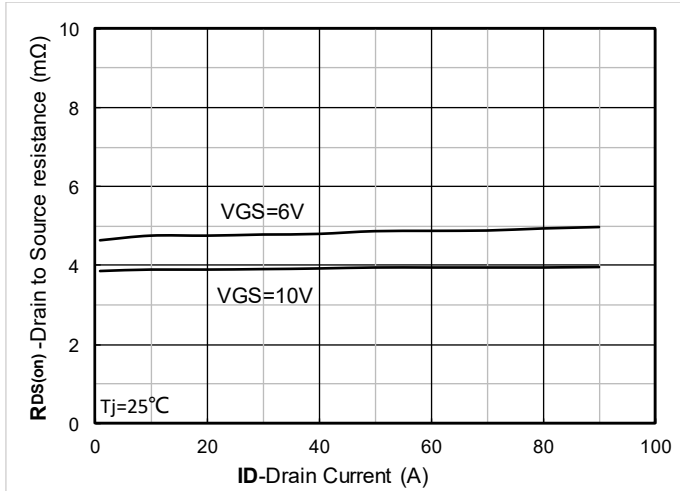


Figure7. RDS(on) VS Drain Current

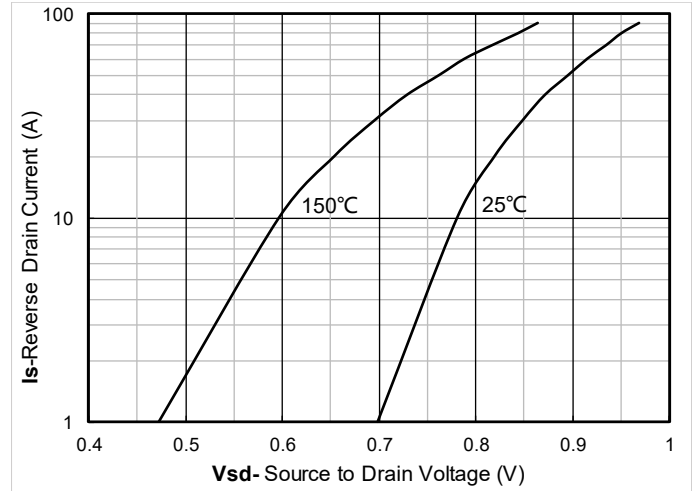


Figure8. Forward characteristics of reverse diode

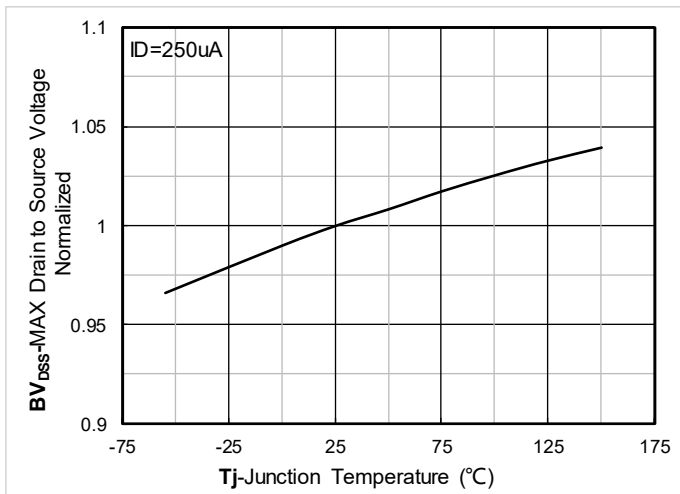


Figure9. Normalized breakdown voltage

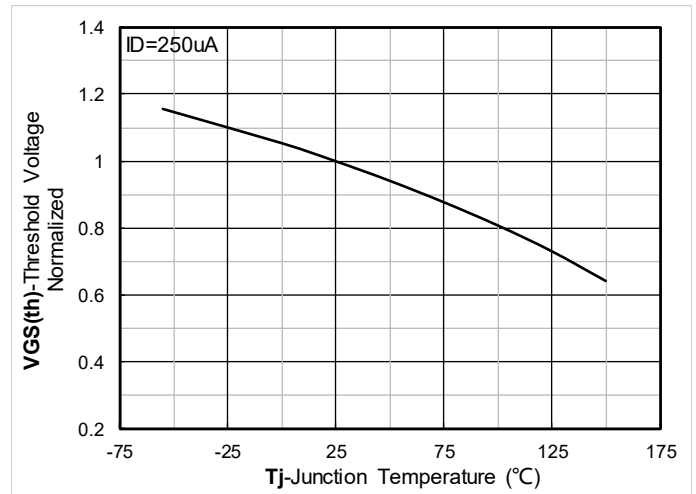


Figure10. Normalized Threshold voltage

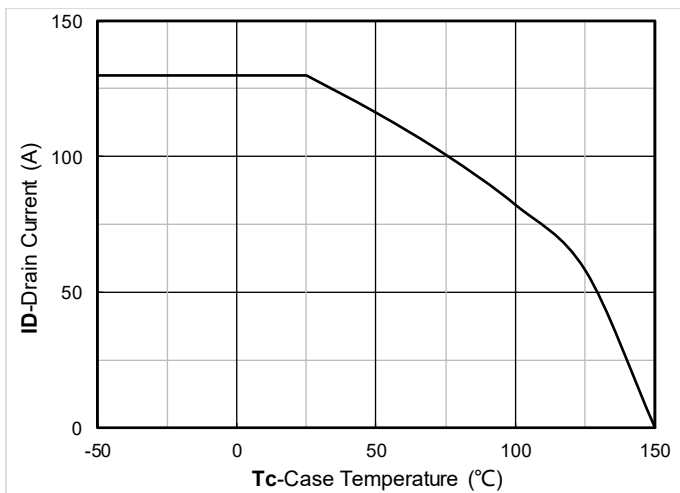


Figure11. Current dissipation

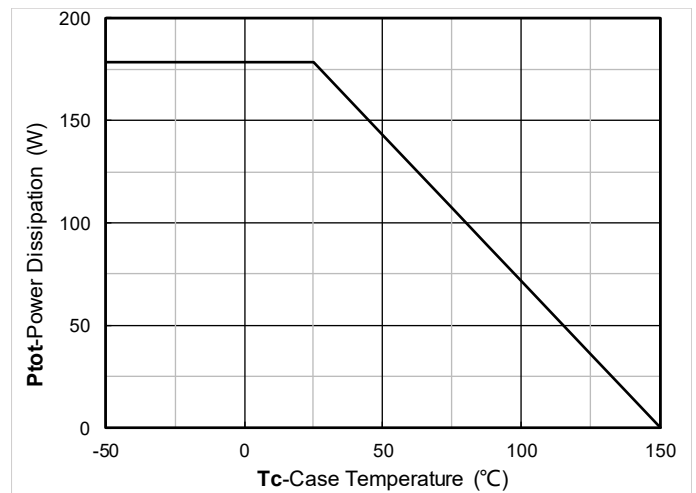


Figure12. Power dissipation

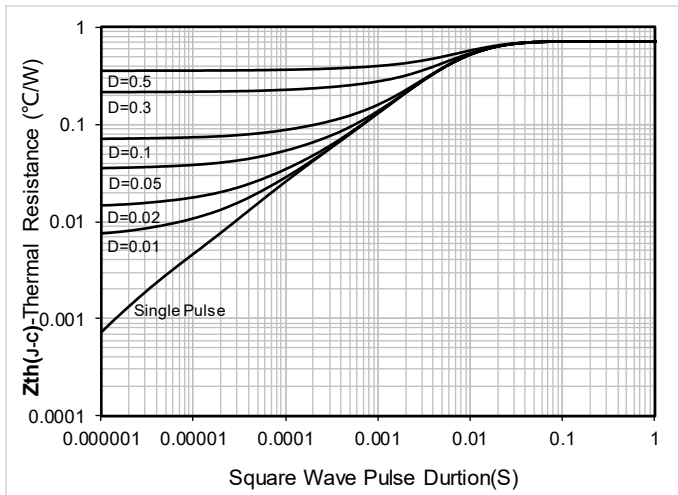


Figure13. Maximum Transient Thermal Impedance

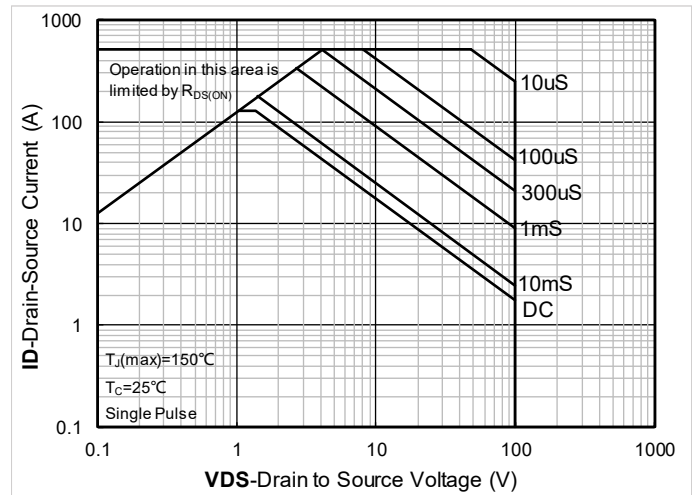


Figure14. Safe Operation Area

■ Test Circuits & Waveforms

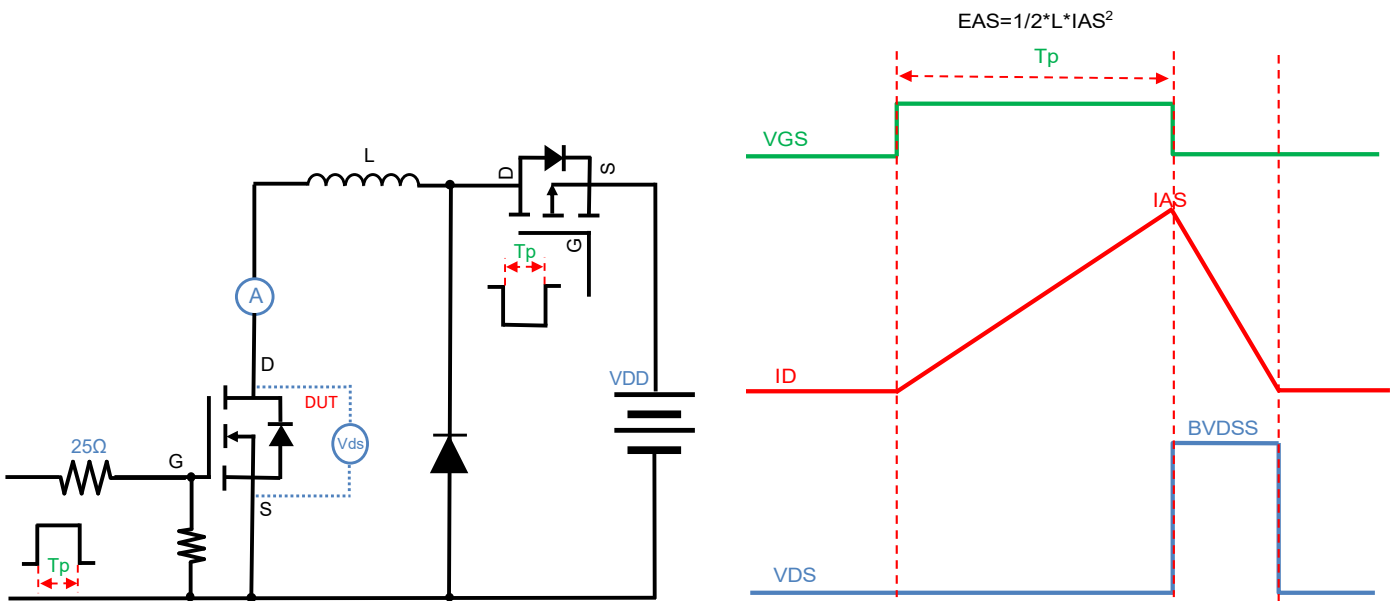


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

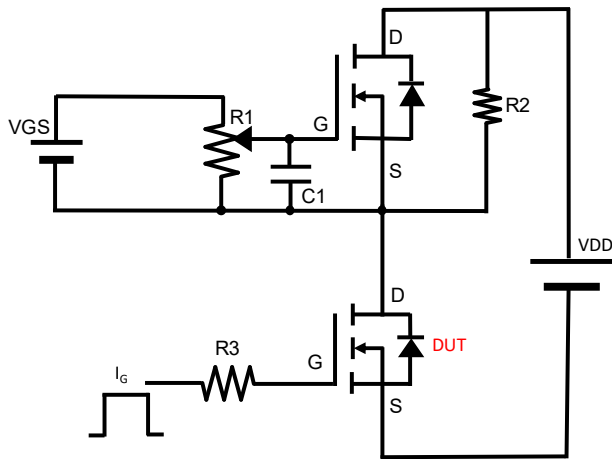


Figure B. Gate Charge Test Circuit & Waveform

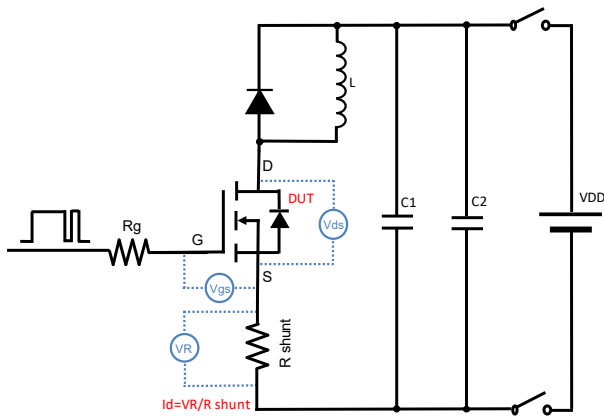


Figure C. Resistive Switching Test Circuit & Waveform

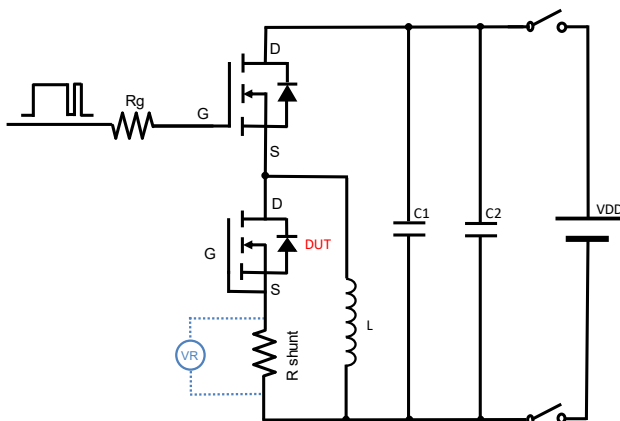
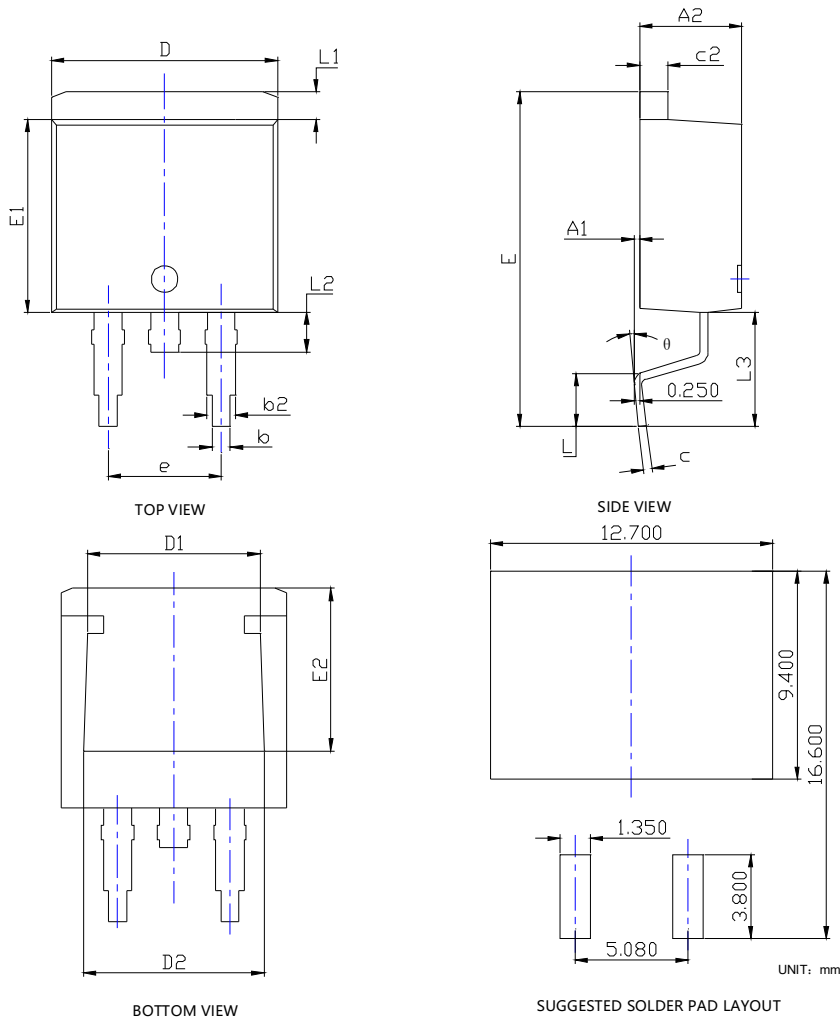


Figure D. Diode Recovery Test Circuit & Waveform

■ TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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