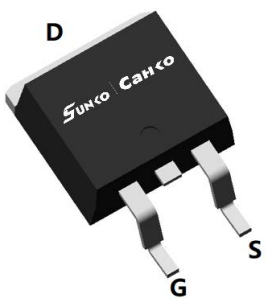
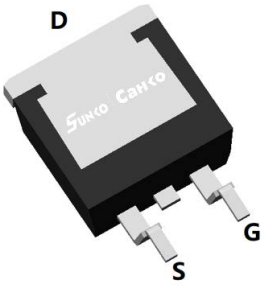
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View

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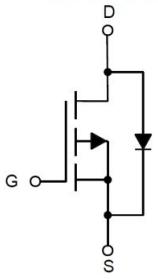


Product Summary

- V_{DS} 100V
- I_D 70A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜8.6 mohm
- $R_{DS(ON)}$(at V_{GS}=6V) ＜13 mohm
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Hard switched and high frequency circuits
- UPS

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current [A] (Package Limited)	T_A=25℃	I_D	10	A
	T_A=100℃		6	
	T_C=25℃		70	
	T_C=100℃		44	
Pulsed Drain Current [B]		I_{DM}	280	A
Avalanche energy [C]		E_{AS}	200	mJ
Total Power Dissipation [D]	T_A=25℃	P_D	2	W
	T_A=100℃		0.8	
	Tc=25℃		125	
	Tc=100℃		50	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [E]	t≤10S	$R_{\theta JA}$	12	15	℃/W
Thermal Resistance Junction-to-Ambient [E]	Steady-State		50	60	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1.0	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCB70G10B	F2	SCB70G10B	800	/	8000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100,V_{GS}=0V			1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150℃			100	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	2.8	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		7.2	8.6	mΩ
		V_{GS}= 6V, I_D=20A		10	13	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				70	A
Gate resistance	R_G	f= 1 MHz		0.68		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		2270		pF
Output Capacitance	C_{oss}			797		
Reverse Transfer Capacitance	C_{rss}			36		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=25A		32		nC
Gate-Source Charge	Q_{gs}			11.1		
Gate-Drain Charge	Q_{gd}			4.78		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		84		
Reverse Recovery Time	t_{rr}			51.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V,I_D=25A R_{GEN}=2.2Ω		51		
Turn-on Rise Time	t_r			14.4		
Turn-off Delay Time	$t_{D(off)}$			69.2		
Turn-off fall Time	t_f			20.6		

A. The maximum current rating is package limited.
B. Repetitive rating; pulse width limited by max. junction temperature.
C. V_{DD}=50V, R_G=25Ω, L=0.5mH, starting T_J=25 ℃.
D. Pd is based on max. junction temperature, using junction-case thermal resistance.
E. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PDSM is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

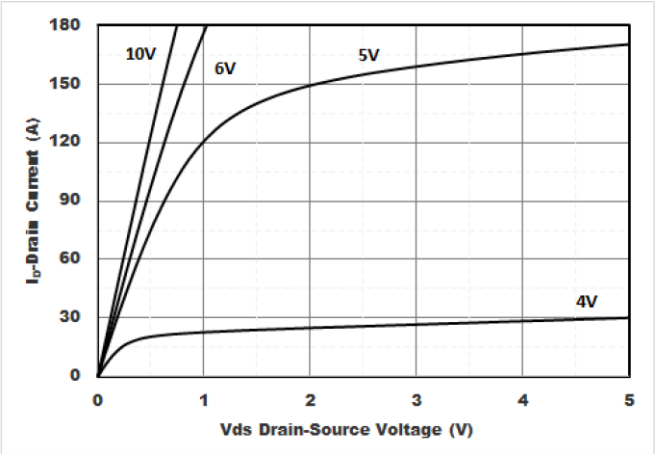


Figure1. Output Characteristics

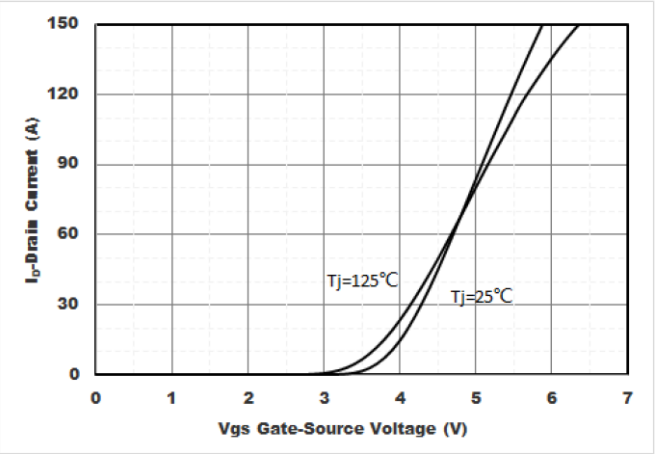


Figure2. Transfer Characteristics

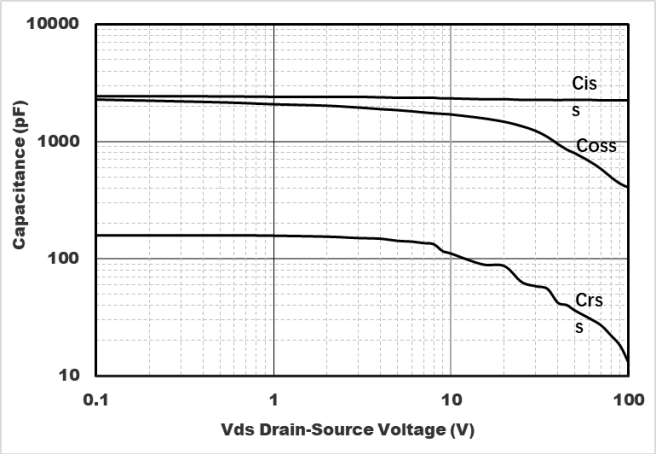


Figure3. Capacitance Characteristics

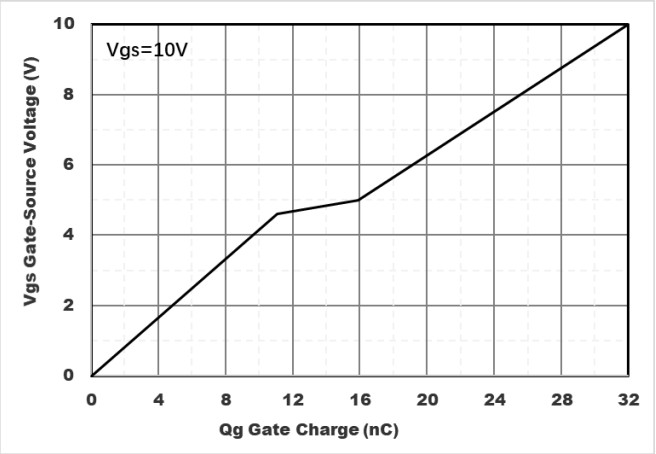


Figure4. Gate Charge

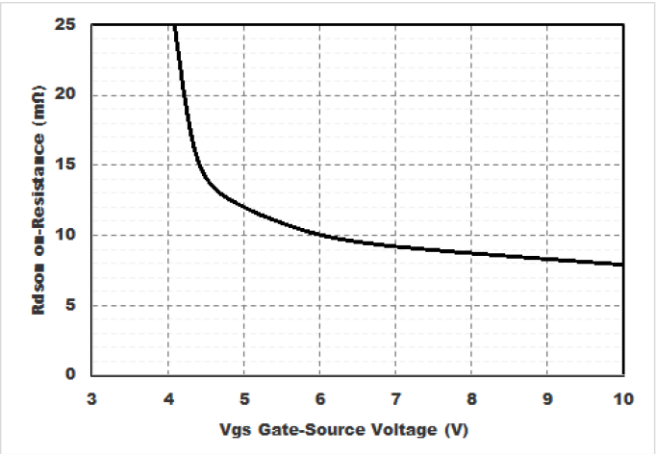


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

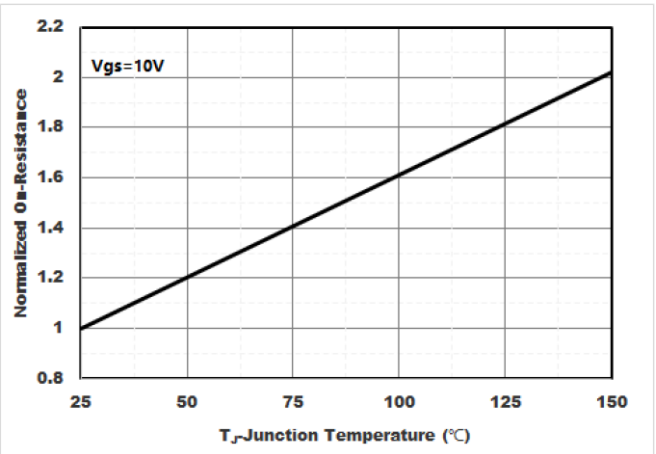


Figure6.Normalized On-Resistance

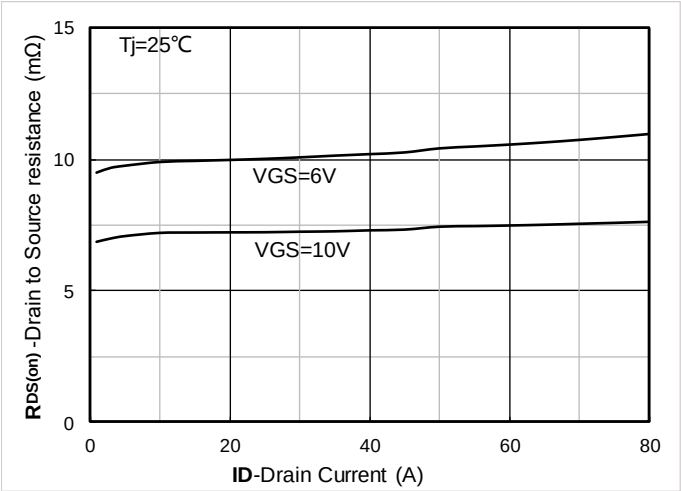


Figure 7. $R_{DS(on)}$ VS Drain Current

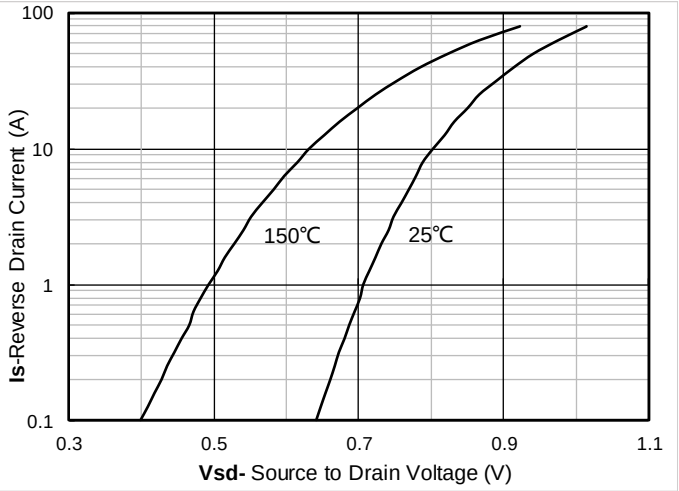


Figure 8. Forward characteristics of reverse diode

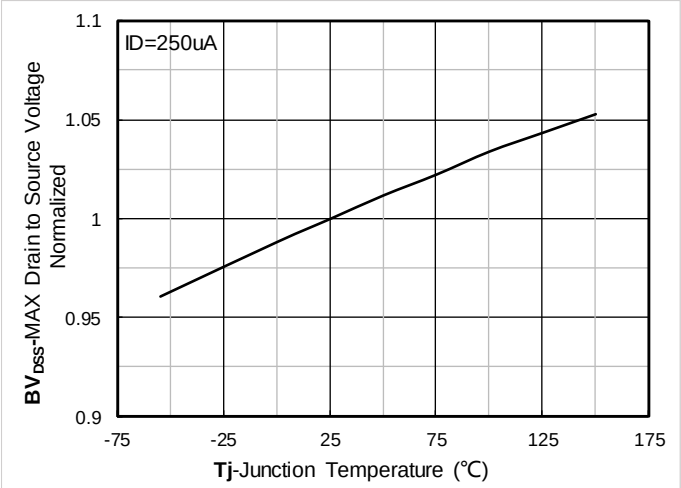


Figure 9. Normalized breakdown voltage

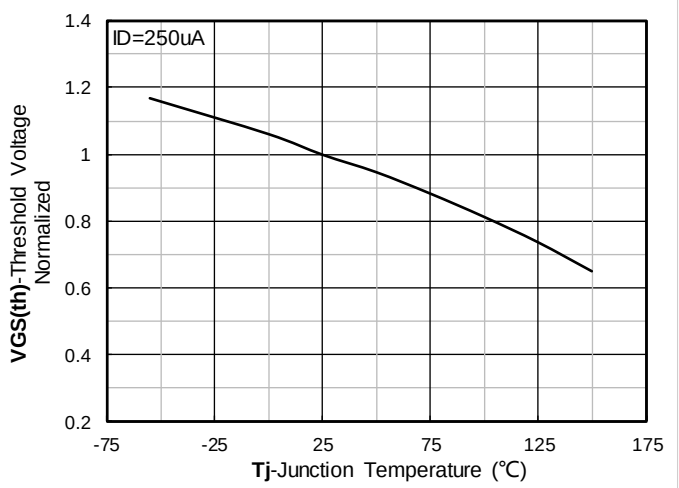


Figure 10. Normalized Threshold voltage

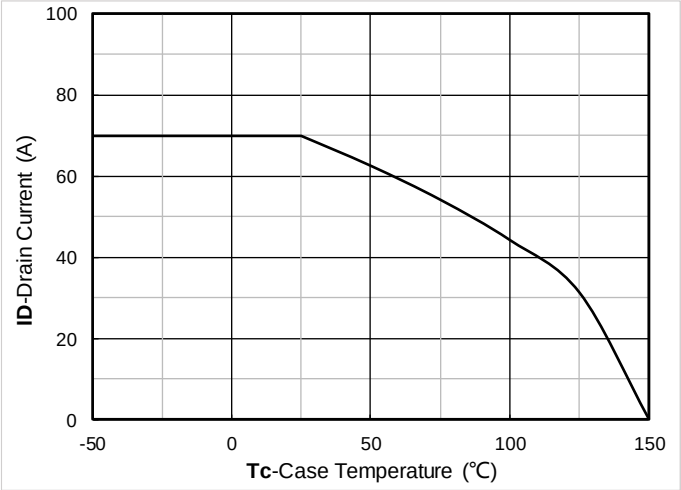


Figure 11. Current dissipation

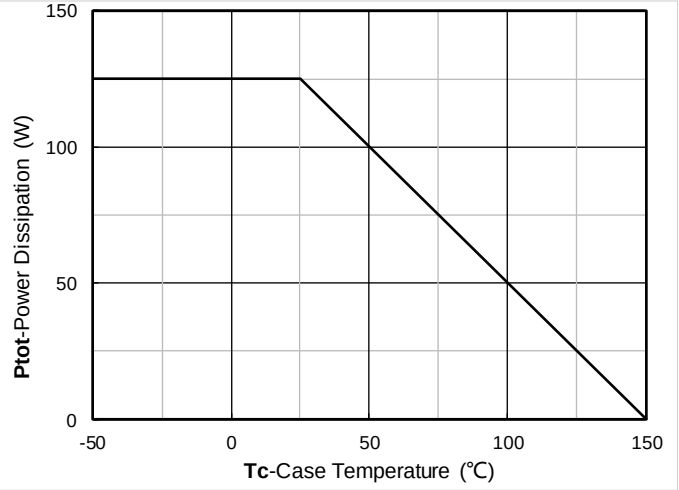


Figure 12. Power dissipation

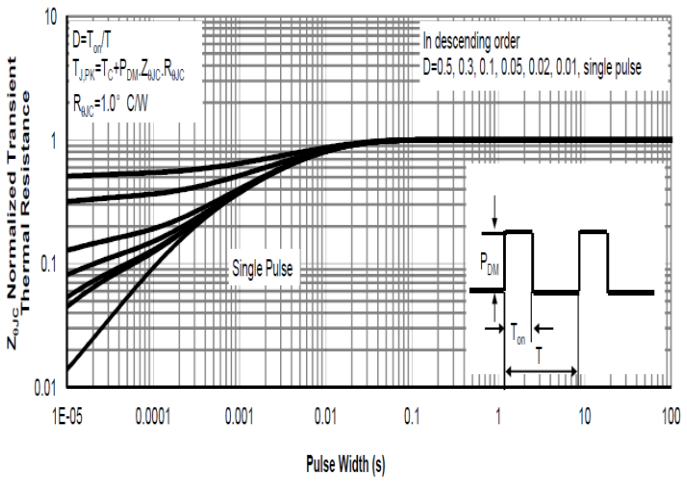


Figure 13. Normalized Maximum Transient thermal impedance

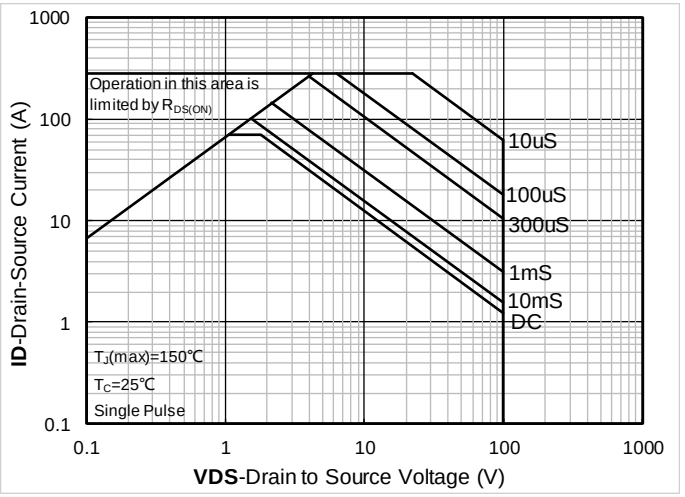
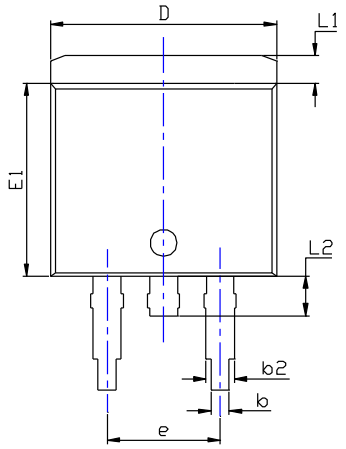
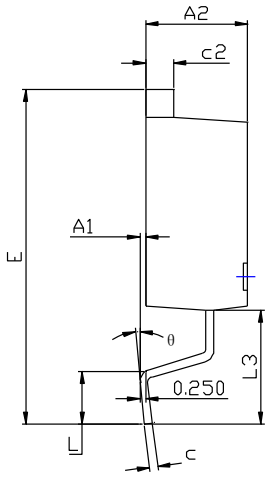


Figure 14. Safe Operation Area

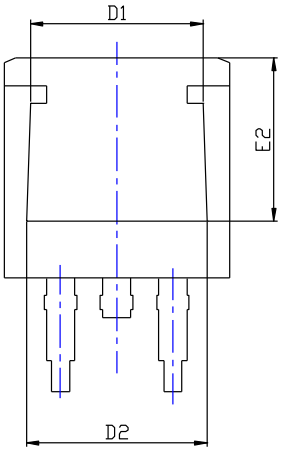
■ TO-263-HY Package information



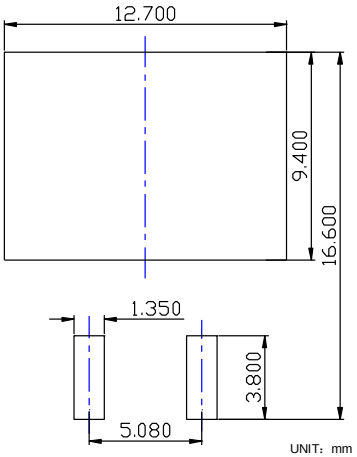
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS						
SYMBOL	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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