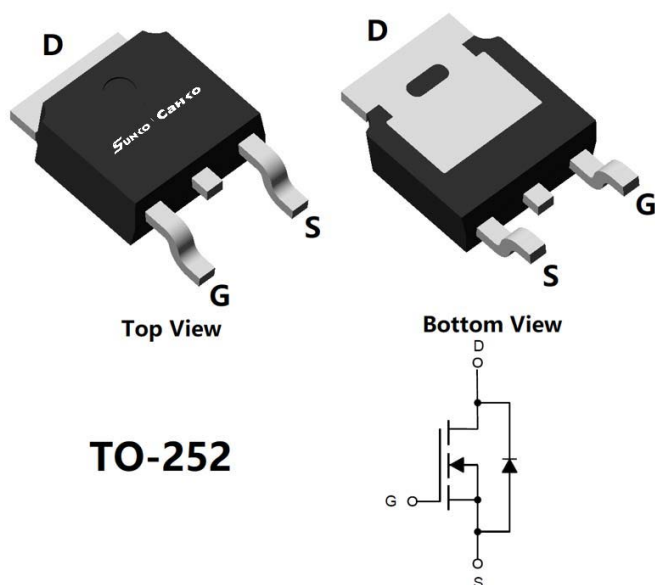


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	-100V
• I_D	-28A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	<58 mohm
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	<65 mohm
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load Switch
- Battery Protection

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_c=25^{\circ}C$	I_D	-28	A
	$T_c=100^{\circ}C$		-17.8	
Pulsed Drain Current ^A		I_{DM}	-112	A
Avalanche energy ^B		E_{AS}	220	mJ
Total Power Dissipation	$T_c=25^{\circ}C$	P_D	96	W
	$T_c=100^{\circ}C$		38	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	16	20	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1	1.3	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCD28GP10A	F1/F2	SCD28GP10A	2500	2500	25000	13" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA		-100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	T _J =25℃			-1	μA
			T _J =55℃			-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V				±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA		-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D =-15A			42	58	mΩ
		V _{GS} = -4.5V, I _D =-7A			46	65	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V				-1.3	V
Maximum Body-Diode Continuous Current	I _S					-28	A
Dynamic Parameters							
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHZ			2100		pF
Output Capacitance	C _{oss}				236		
Reverse Transfer Capacitance	C _{rss}				48		
Switching Parameters							
Total Gate Charge	Q _g (-10V)	V _{GS} =-10V, V _{DS} =-50V, I _D =-5A			40		nC
Total Gate Charge	Q _g (-4.5V)				19.4		
Gate-Source Charge	Q _{gs}				7.8		
Gate-Drain Charge	Q _{gd}				8.6		
Reverse Recovery Charge	Q _{rr}	I _F =-5A, di/dt=100A/us			280		ns
Reverse Recovery Time	t _{rr}				104		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _{DS} =-5A R _{GEN} =6Ω			13		
Turn-on Rise Time	t _r				39		
Turn-off Delay Time	t _{D(off)}				100.1		
Turn-off fall Time	t _f				105.3		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=1mH, I_{AS}=31A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design

■ Typical Performance Characteristics

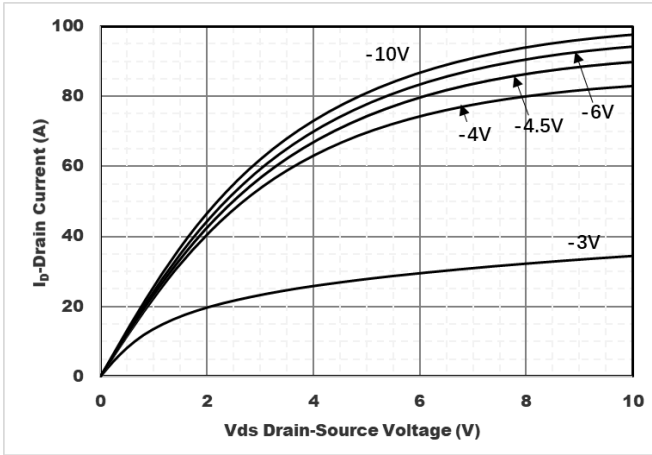


Figure1. Output Characteristics

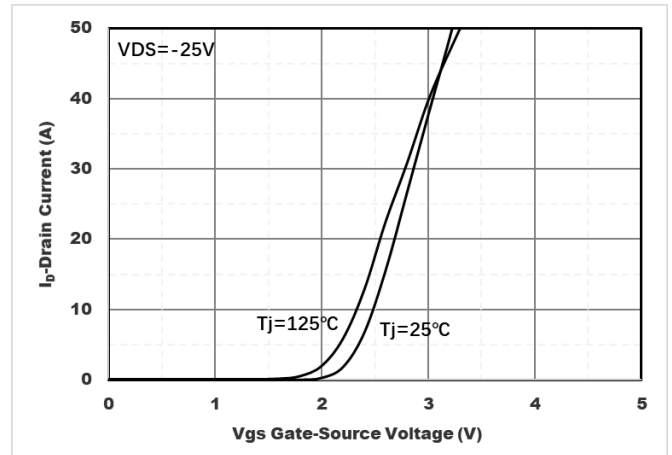


Figure2. Transfer Characteristics

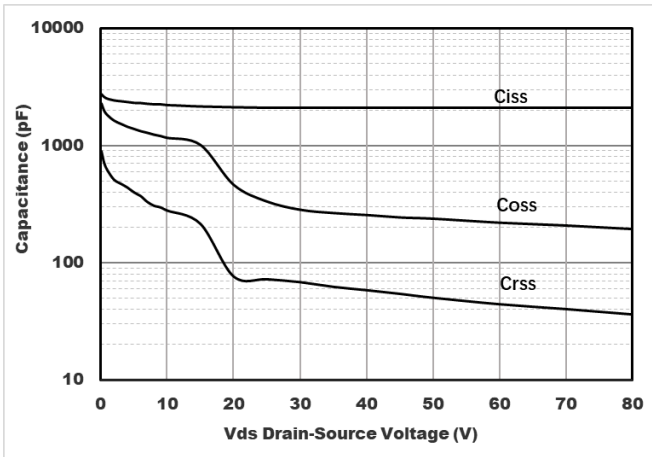


Figure3. Capacitance Characteristics

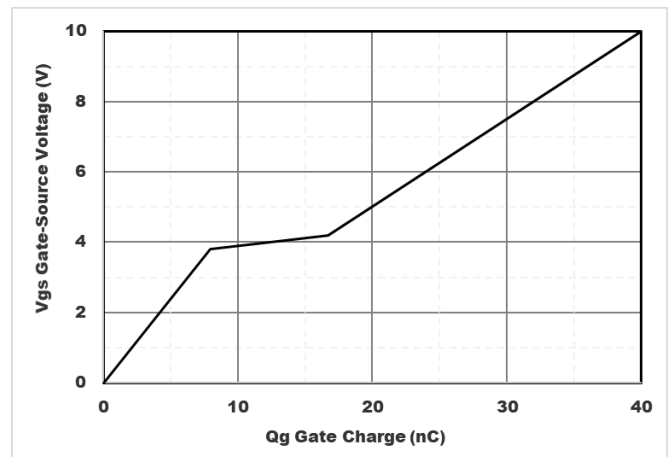


Figure4. Gate Charge

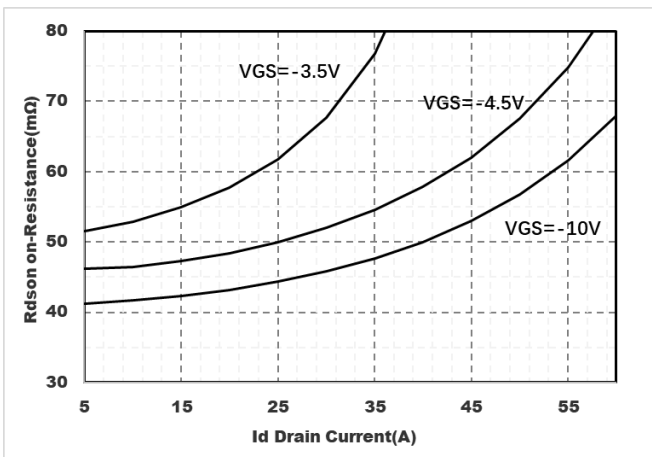


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

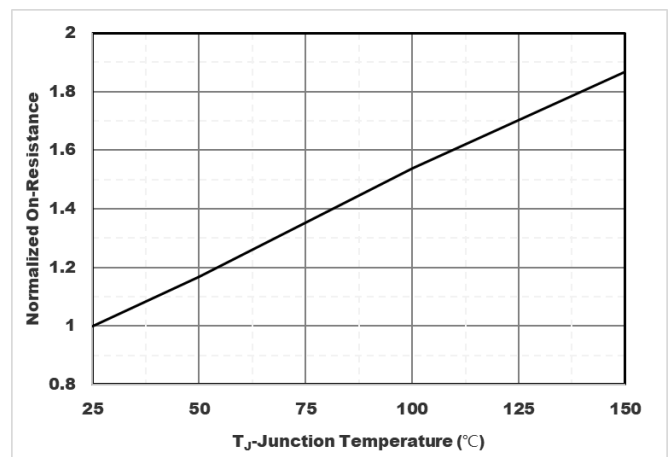


Figure6. Normalized On-Resistance

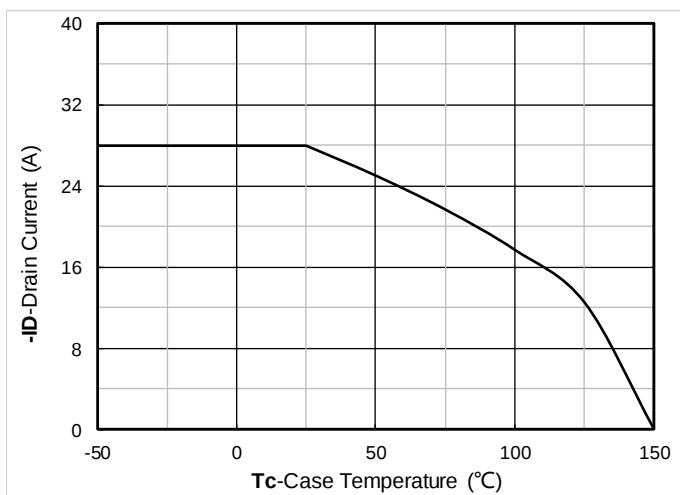


Figure7. Drain current

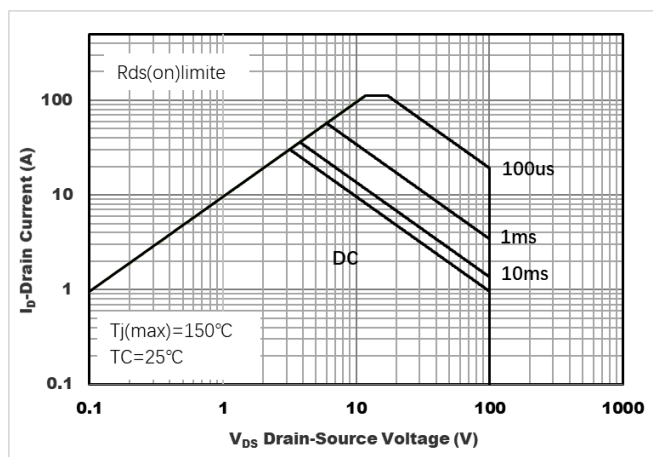


Figure8.Safe Operation Area

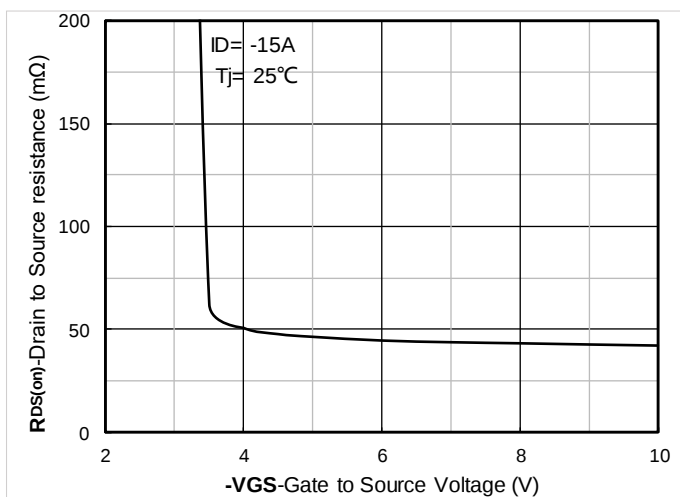


Figure 9. On-Resistance vs Gate to Source Voltage

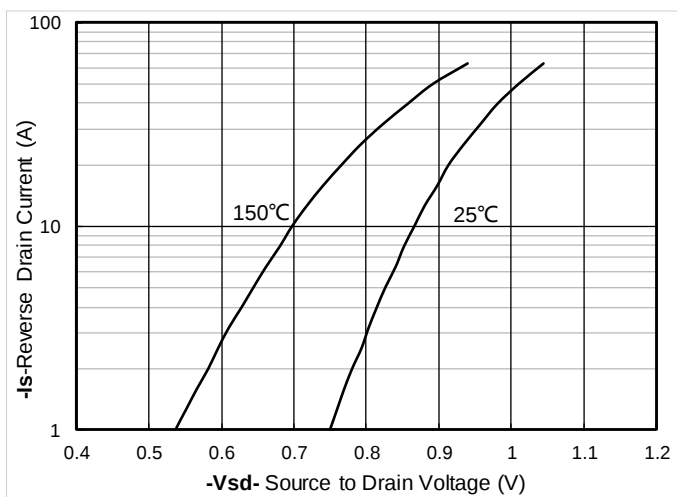


Figure 10. Forward characteristics of reverse diode

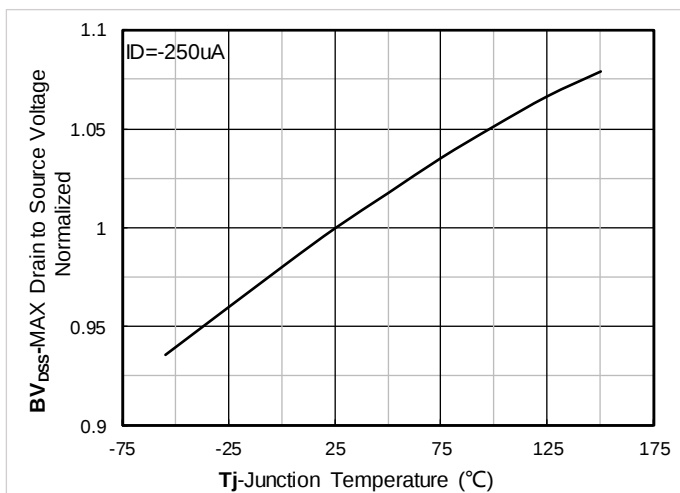


Figure 11. Normalized breakdown voltage

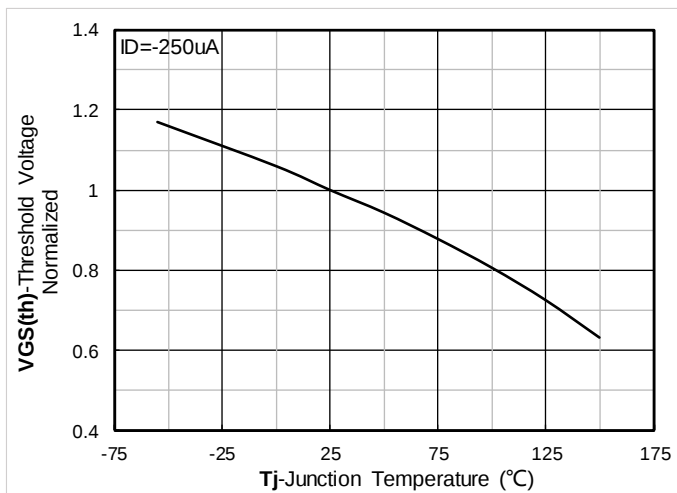


Figure 12. Normalized Threshold voltage

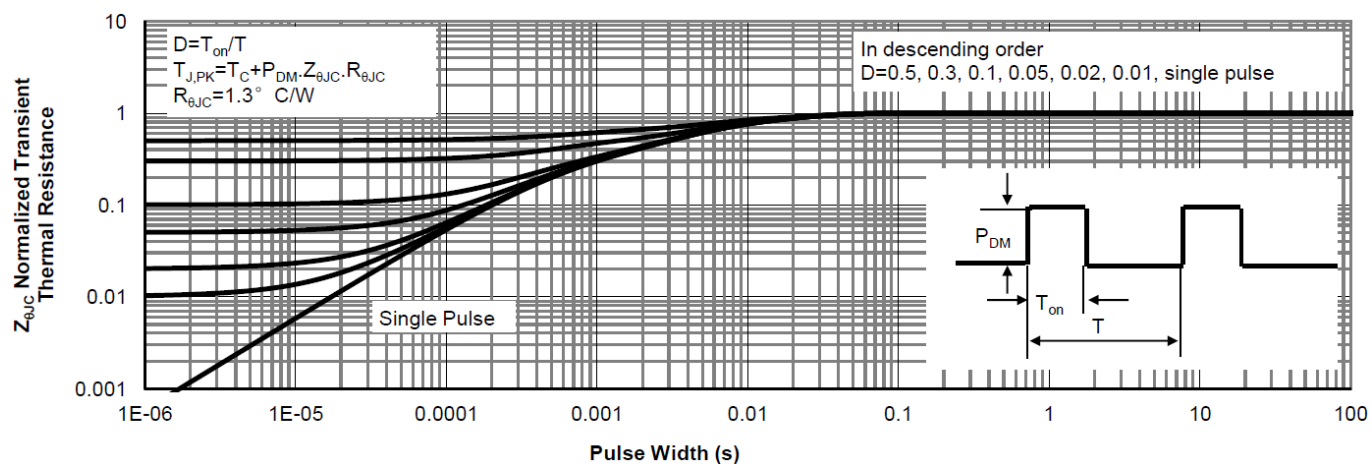
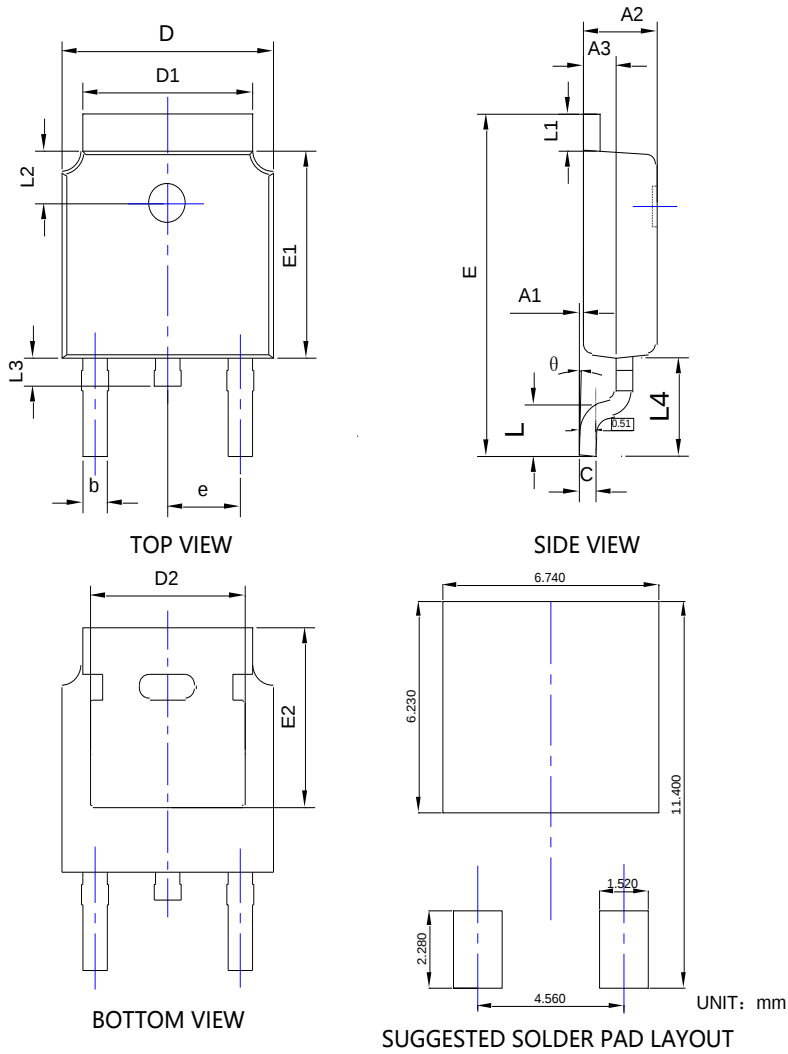


Figure13.Normalized Maximum Transient thermal impedance

■ TO-252-B Package Information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.024	0.031	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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