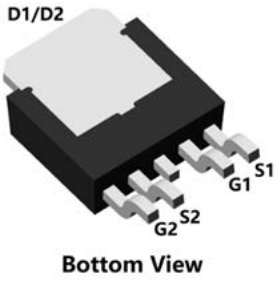
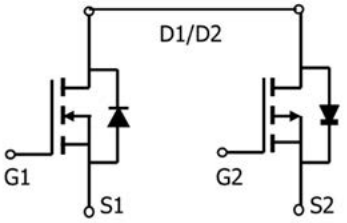
N-Channel and P-Channel Complementary MOSFET

Top View



Bottom View

TO-252-4L



n-channel p-channel

Product Summary

NMOS

- V_{DS} 30V
- I_D 50A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜8.1mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜12.6mΩ

PMOS

- V_{DS} -30V
- I_D -30A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜18mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜28mΩ
- 100% EAS Tested
- 100% $\triangledown V_{DS}$ Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter				Symbol	NMOS	PMOS	Unit
Drain-source Voltage				V_{DS}	30	-30	V
Gate-source Voltage				V_{GS}	±20	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	NMOS: V_{GS}=10V	I_D	13.7	-9.4	A
			PMOS: V_{GS}=-10V				
		T_A=100℃	NMOS: V_{GS}=10V		8.6	-5.9	
			PMOS: V_{GS}=-10V				
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃	NMOS: V_{GS}=10V		50	-30	
			PMOS: V_{GS}=-10V				
		T_C =100℃	NMOS: V_{GS}=10V		31.6	-19	
			PMOS: V_{GS}=-10V				
Pulsed Drain Current	T_C=25℃, t_p=100μs			I_{DM}	200	-120	A
Avalanche energy	NMOS: V_G=10V, R_G=25Ω, L=0.5mH, IAS=10.5A			EAS	27.5	30.2	mJ
	PMOS: V_G=-10V, R_G=25Ω, L=0.5mH, IAS=-11A						
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃		P_D	2.5	2.5	W
		T_A=100℃			1	1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃			35.7	29.7	
		T_C =100℃			14.2	11.9	
Junction and Storage Temperature Range				T_J , T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	40	50	40	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.9	3.5	3.5	4.2	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCD35NP03B	F1/F2	SCD35NP03B	2500	/	25000	13"Reel

■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	μA
		V_{DS}=30V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	6.2	8.1	mΩ
		V_{GS}=4.5V, I_D=20A	-	9.3	12.6	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	2.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	50	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	1016	-	pF
Output Capacitance	C_{oss}		-	176	-	
Reverse Transfer Capacitance	C_{rss}		-	150	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=15V, I_D=20A	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us	-	0.66	-	nC
Reverse Recovery Time	t_{rr}		-	10	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=15V, I_D=20A R_{GEN}=3Ω	-	11	-	ns
Turn-on Rise Time	t_r		-	55	-	
Turn-off Delay Time	$t_{D(off)}$		-	27	-	
Turn-off fall Time	t_f		-	66	-	

■ PMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-30V, V_{GS}=0V, Tj=150℃	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-20A	-	14	18	mΩ
		V_{GS}=-4.5V, I_D=-20A	-	21	28	
Diode Forward Voltage	V_{SD}	I_S=-20A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	15	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-30	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz	-	1210	-	pF
Output Capacitance	C_{oss}		-	180	-	
Reverse Transfer Capacitance	C_{rss}		-	150	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-15V, I_D=-10A	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Reverse Recovery Charge	Q_{rr}	I_F=-10A, di/dt=100A/us	-	11	-	nC
Reverse Recovery Time	t_{rr}		-	35	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-15V, ID=-10A R_{GEN}=2.5Ω	-	11	-	ns
Turn-on Rise Time	t_r		-	4	-	
Turn-off Delay Time	$t_{D(off)}$		-	70	-	
Turn-off fall Time	t_f		-	50	-	

Note:
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

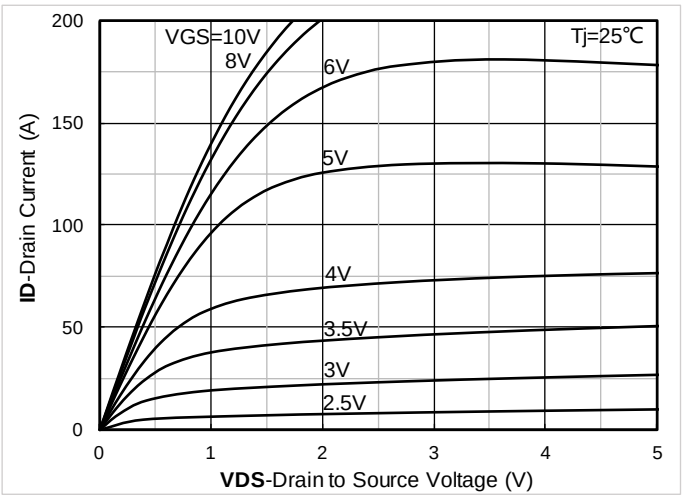


Figure 1. Output Characteristics

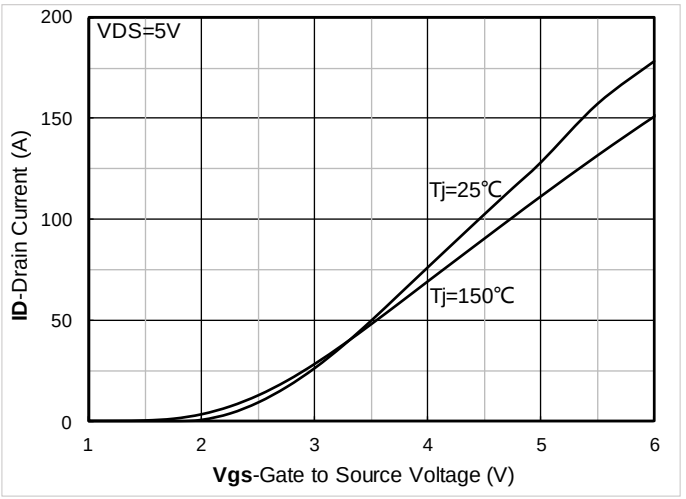


Figure 2. Transfer Characteristics

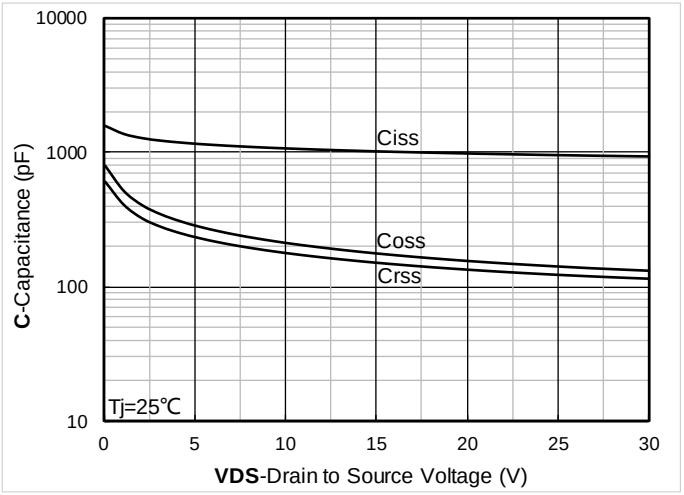


Figure 3. Capacitance Characteristics

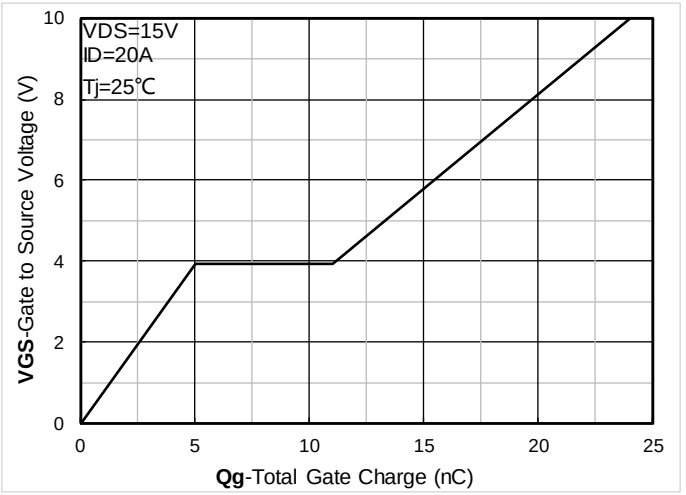


Figure 4. Gate Charge

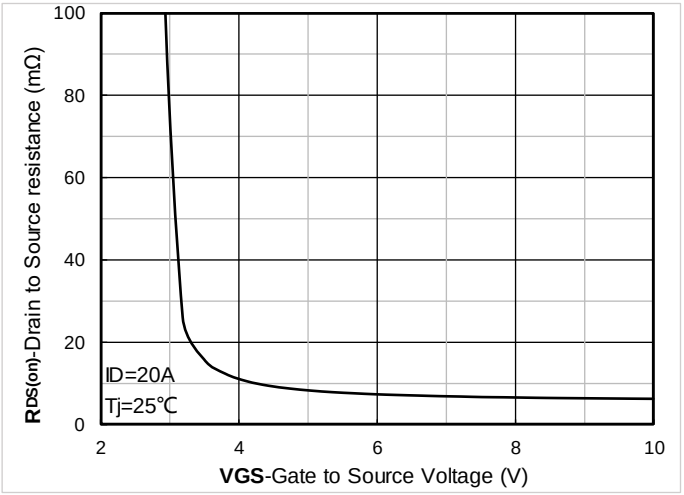


Figure 5. On-Resistance vs Gate to Source Voltage

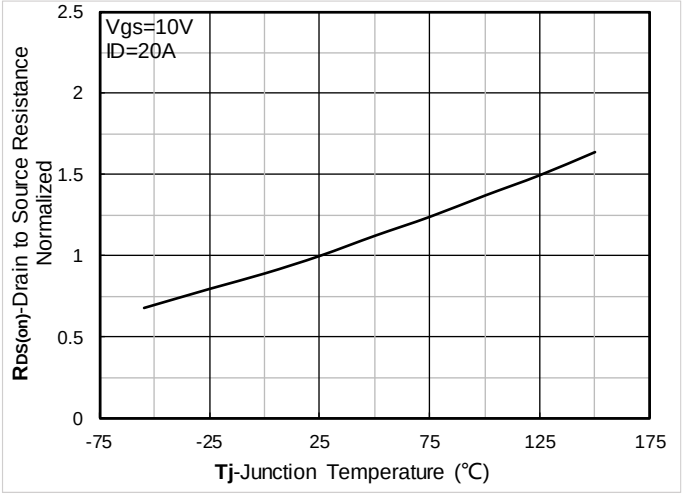


Figure 6. Normalized On-Resistan

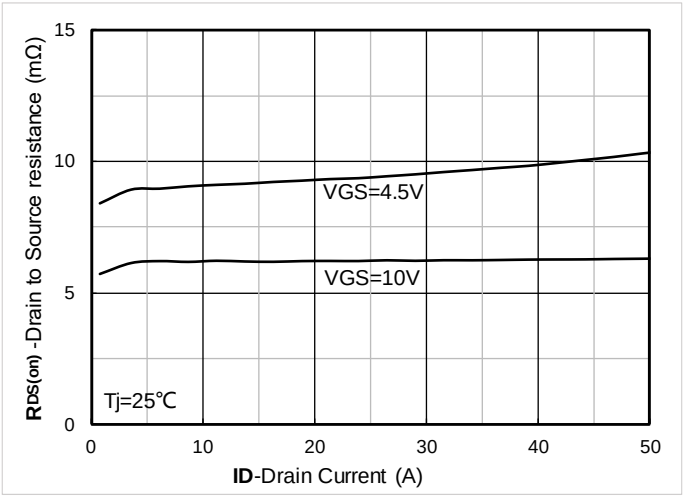


Figure 7. $R_{DS(on)}$ VS Drain Current

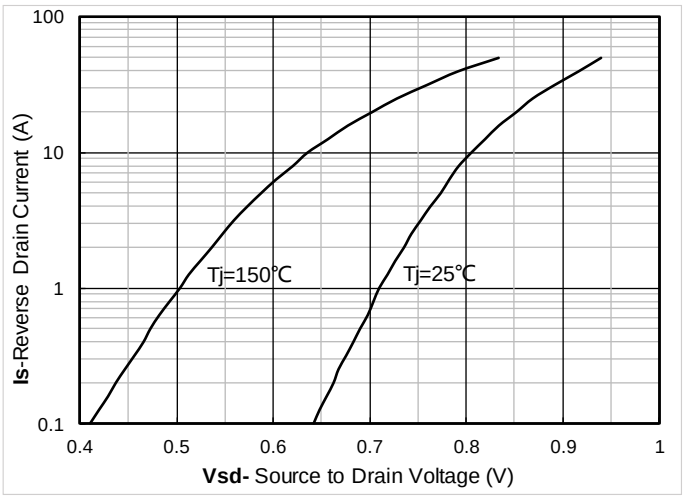


Figure 8. Forward characteristics of reverse diode

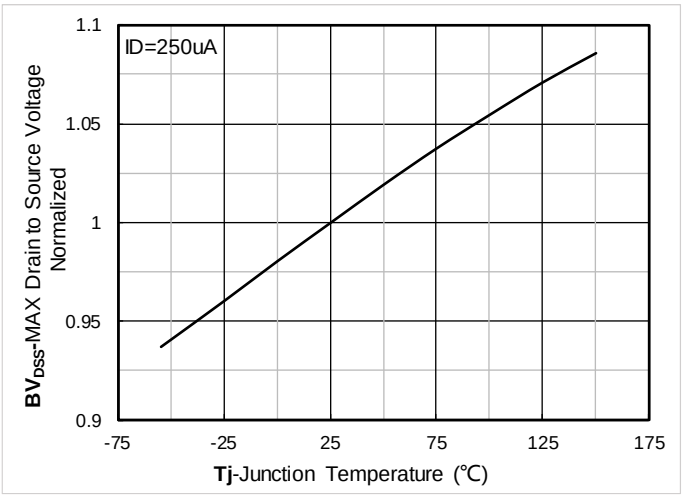


Figure 9. Normalized breakdown voltage

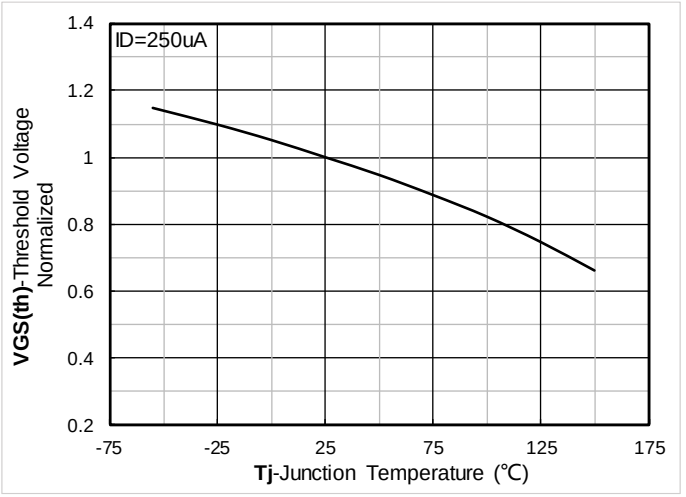


Figure 10. Normalized Threshold voltage

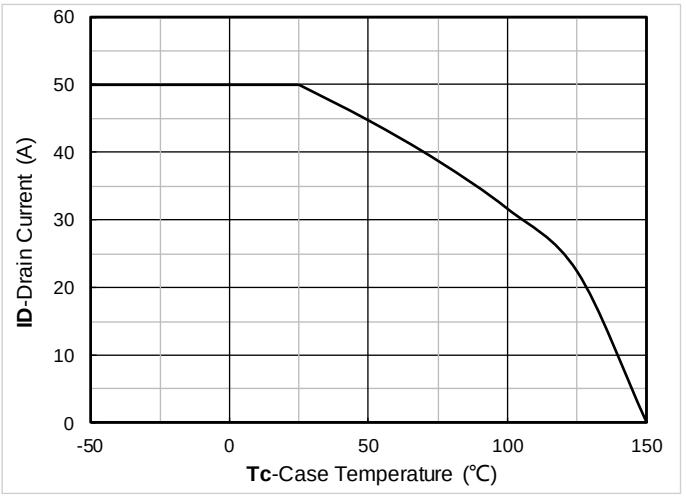


Figure 11. Current dissipation

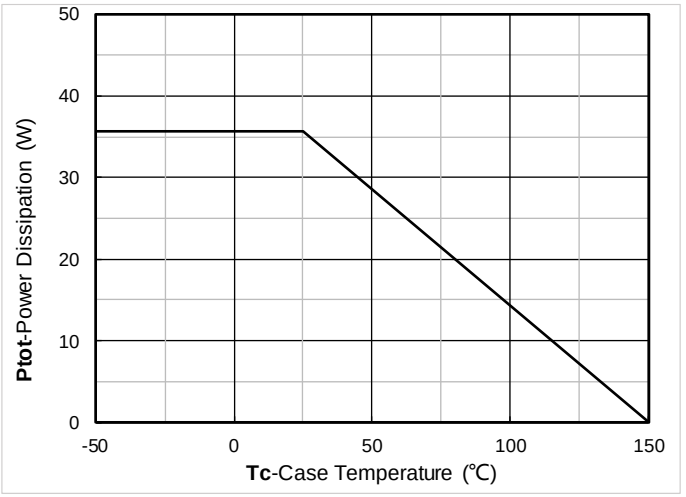


Figure 12. Power dissipation

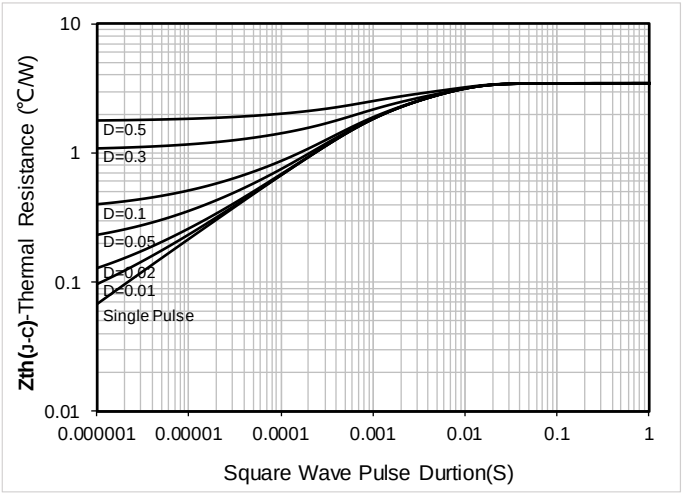


Figure 13. Maximum Transient Thermal Impedance

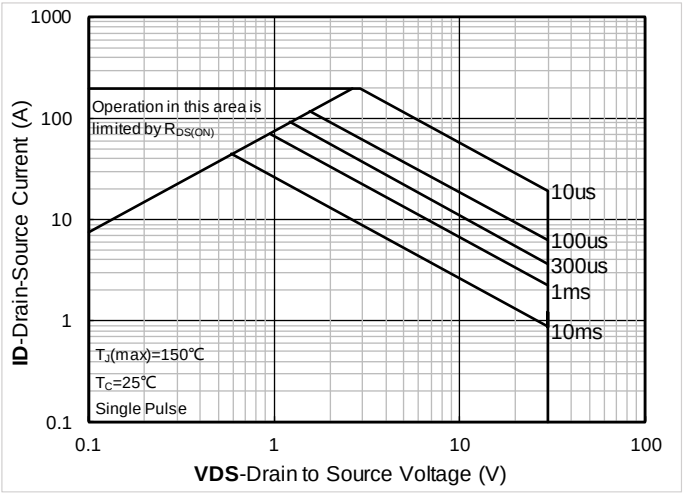


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

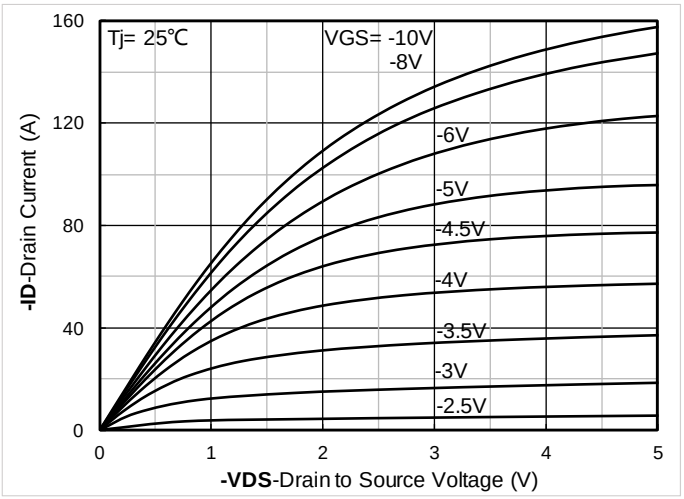


Figure 1. Output Characteristics

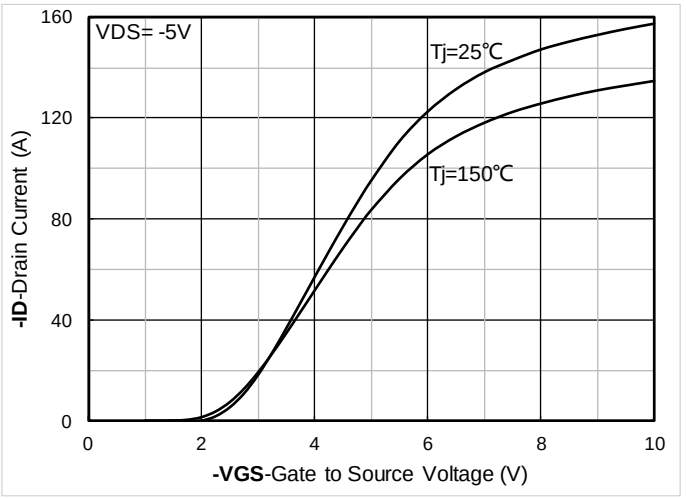


Figure 2. Transfer Characteristics

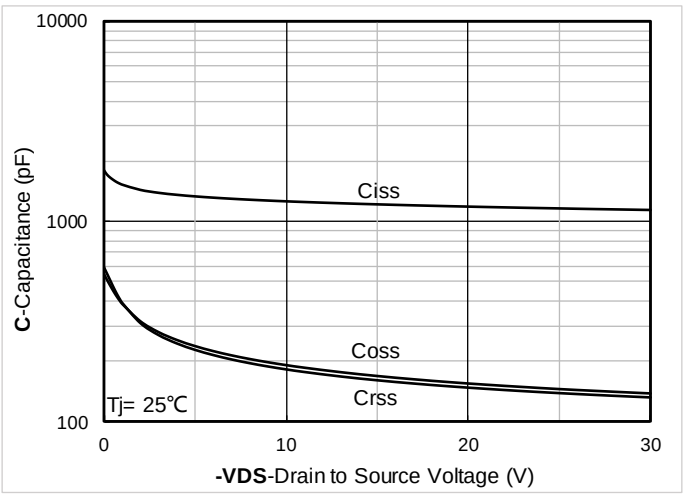


Figure 3. Capacitance Characteristics

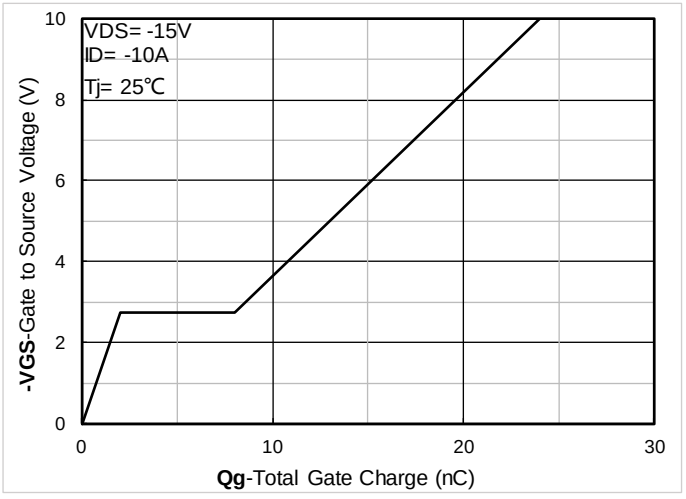


Figure 4. Gate Charge

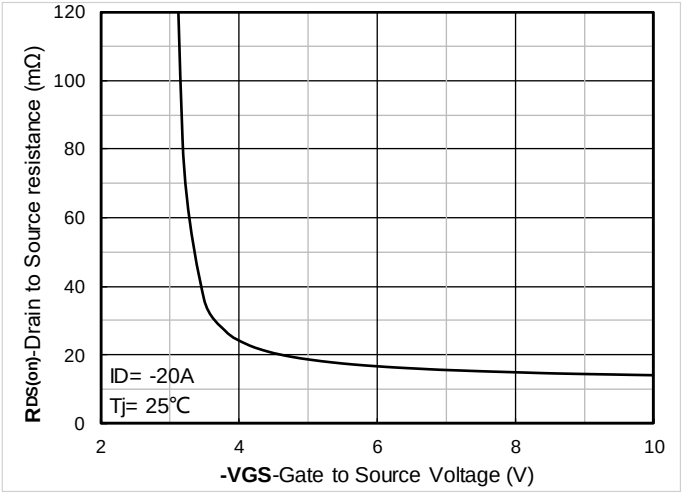


Figure 5. On-Resistance vs Gate to Source Voltage

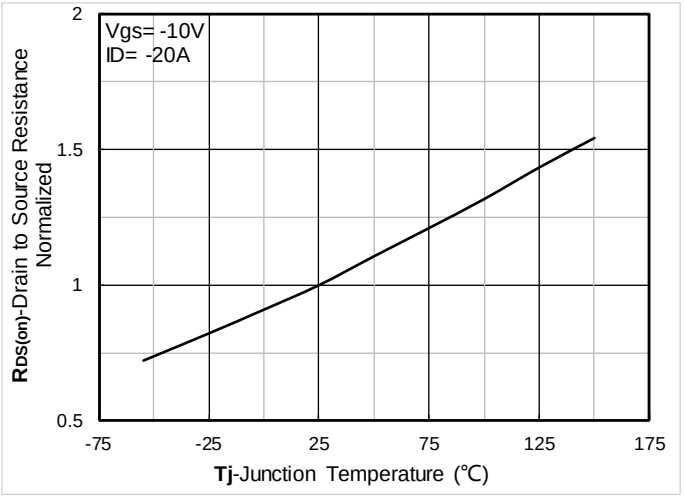


Figure 6. Normalized On-Resistance

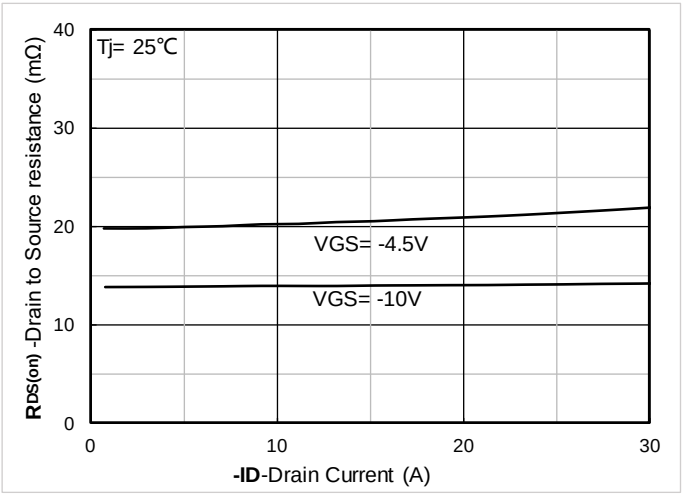


Figure 7. $R_{DS(on)}$ VS Drain Current

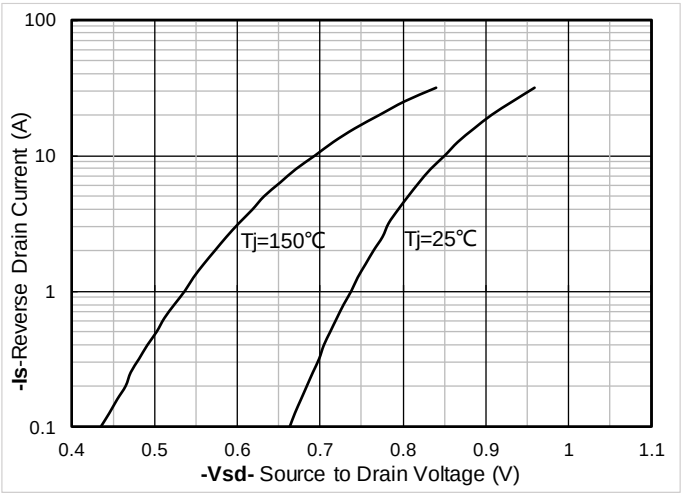


Figure 8. Forward characteristics of reverse diode

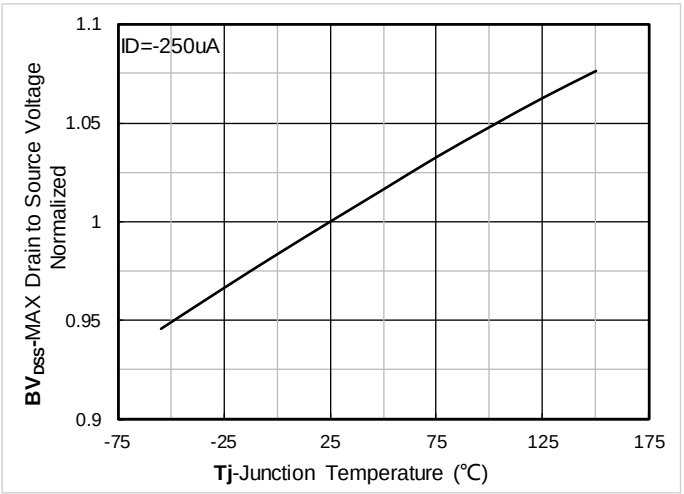


Figure 9. Normalized breakdown voltage

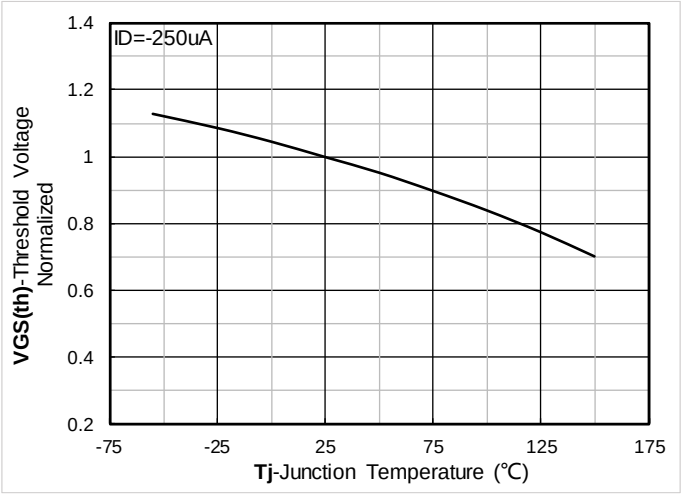


Figure 10. Normalized Threshold voltage

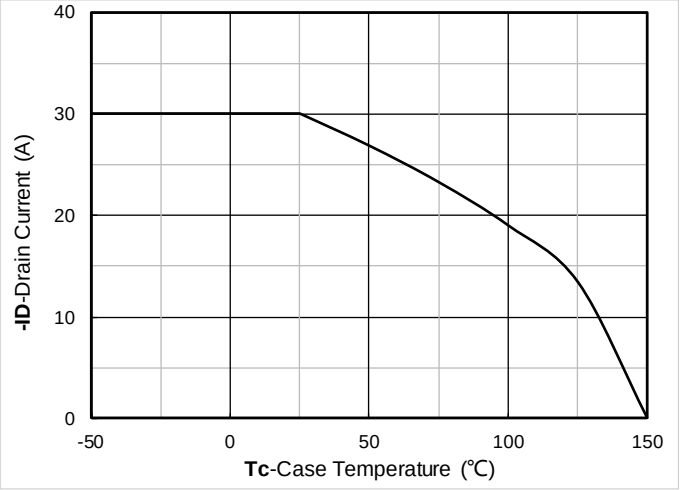


Figure 11. Current dissipation

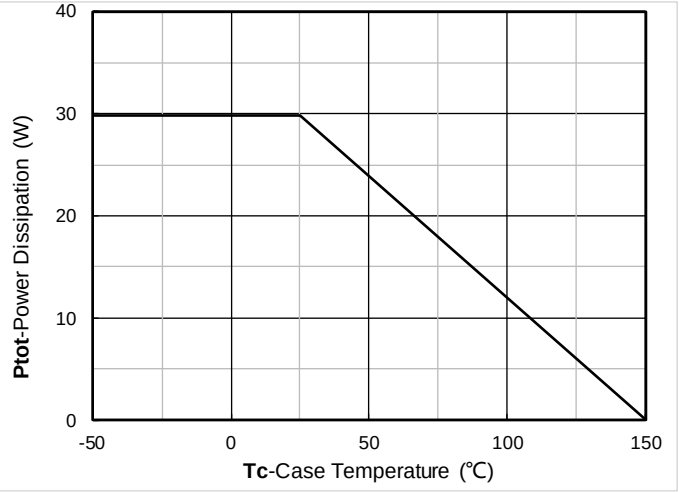


Figure 12. Power dissipation

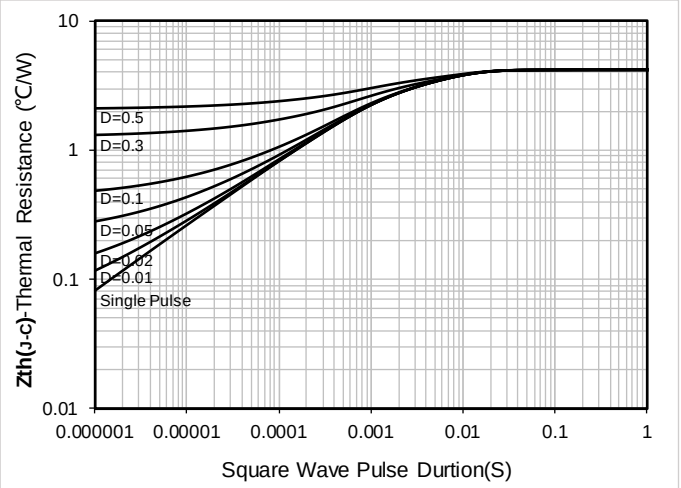


Figure 13. Maximum Transient Thermal Impedance

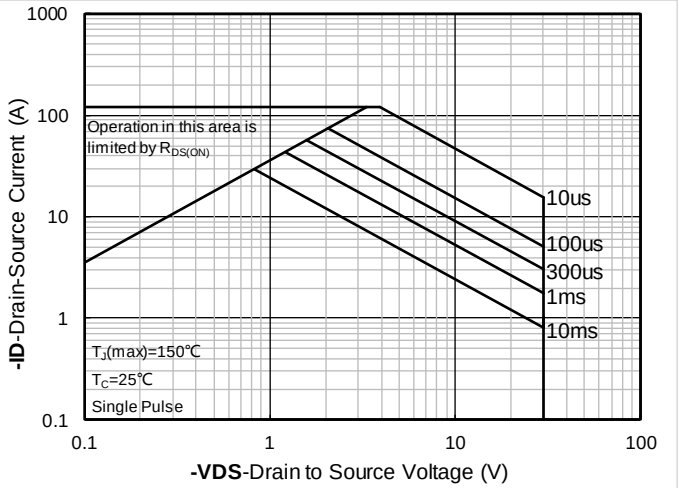
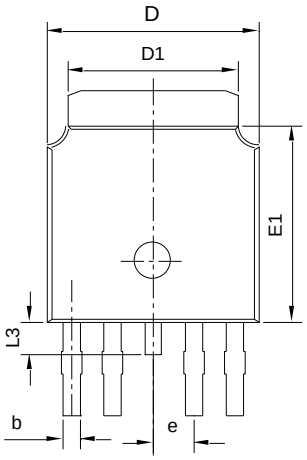
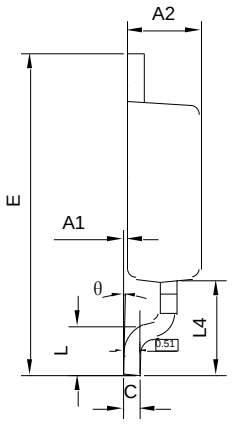


Figure 14. Safe Operation Area

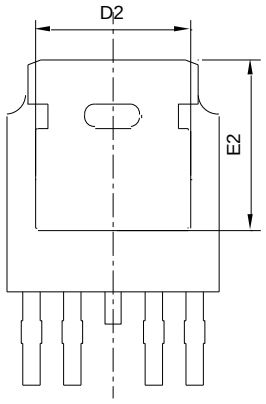
■ TO-252-4L Package information



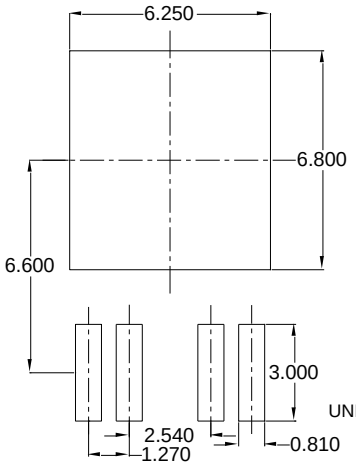
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.000	0.008	0.000	0.200
A2	0.085	0.094	2.150	2.400
b	0.016	0.030	0.400	0.750
c	0.018	0.026	0.450	0.650
D	0.248	0.268	6.300	6.800
D1	0.189	0.217	4.800	5.500
D2	0.150	-	3.800	-
E	0.366	0.413	9.300	10.500
E1	0.213	0.248	5.400	6.300
E2	0.177	-	4.500	-
e	0.050BSC		1.270BSC	
L	0.049	0.073	1.250	1.850
L3	-	0.047	-	1.200
L4	0.108REF		2.740REF	
?	0°	10°	0°	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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