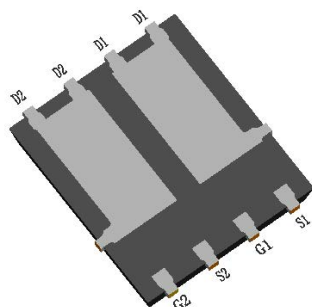
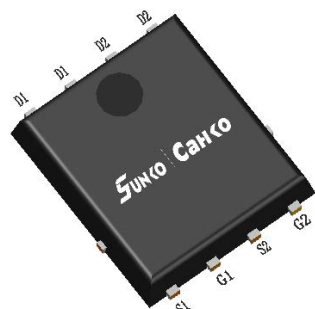
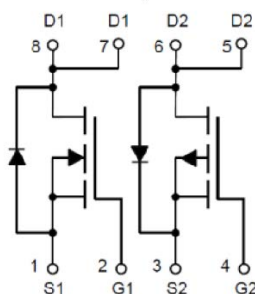


N-Channel and P-Channel Complementary MOSFET



PDFN5060-8L



Product Summary

NMOS

• V_{DS}	60V
• I_D	20A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<32m Ω
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<37m Ω

PMOS

• V_{DS}	-60V
• I_D	-12A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	<110m Ω
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	<135m Ω

- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power Management
- DC Motor Control

■ Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	NMOS	PMOS	Unit
Drain-source Voltage			V_{DS}	60	-60	V
Gate-source Voltage			V_{GS}	± 20	$\$	

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■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
		V _{DS} =60V, V _{GS} =0V, T _J =150℃	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	24	32	mΩ
		V _{GS} =4.5V, I _D =10A	-	27	37	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	1.7	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	20	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz	-	1150	-	pF
Output Capacitance	C _{oss}		-	65	-	
Reverse Transfer Capacitance	C _{rss}		-	55	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	23	-	nC
Gate-Source Charge	Q _{gs}		-	3.8	-	
Gate-Drain Charge	Q _{gd}		-	4.8	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	21	-	nC
Reverse Recovery Time	t _{rr}		-	27	-	ns
Turn-on Delay Time	t _{D(on)}					

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■ PMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-60V, V _{GS} =0V, T _J =150°C	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.2	-1.7	-2.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-12A	-	85	110	mΩ
		V _{GS} =-4.5V, I _D =-6A	-	100	135	
Diode Forward Voltage	V _{SD}	I _S =-12A, V _{GS} =0V	-	-	-1.2	V
Gate resistance	R _G	f=1MHz	-	5.3	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-12	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz	-	900	-	pF
Output Capacitance	C _{oss}		-	44	-	
Reverse Transfer Capacitance	C _{rss}		-	34	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-12A	-	17.3	-	nC
Gate-Source Charge	Q _{gs}		-	1.7	-	
Gate-Drain Charge	Q _{gd}		-	2.7	-	
Reverse Recovery Charge	Q _{rr}	I _F =-12A, di/dt=100A/us	-	21.3	-	nC
Reverse Recovery Time	t _{rr}		-	20.6	-	ns

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

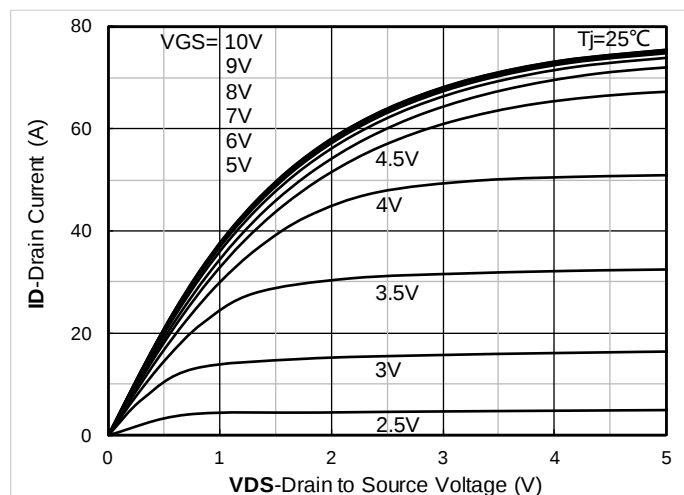


Figure 1. Output Characteristics

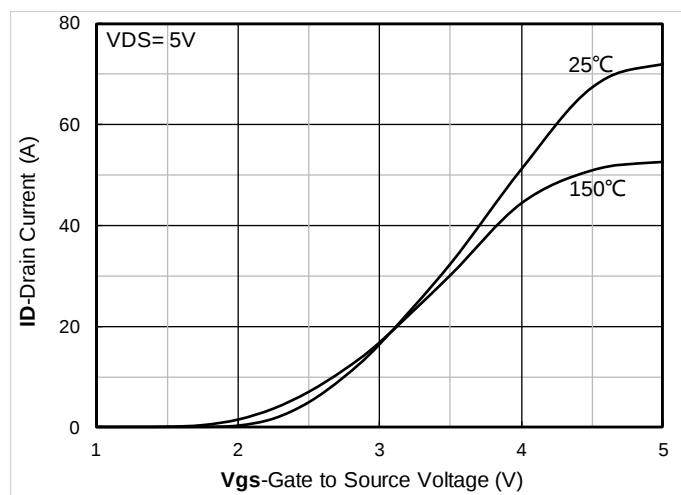


Figure 2. Transfer Characteristics

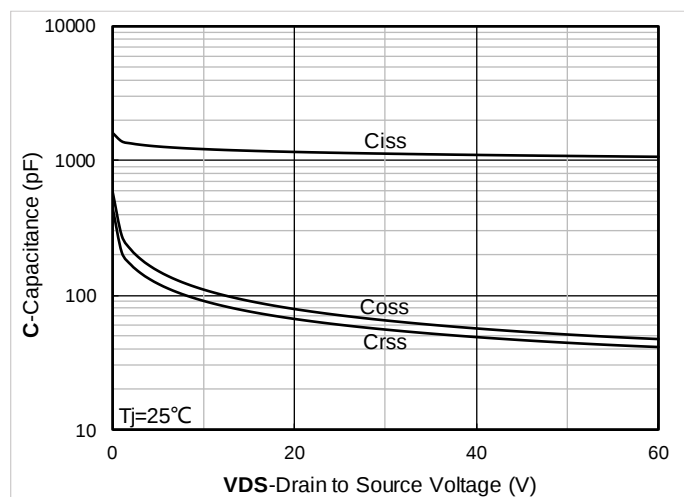


Figure 3. Capacitance Characteristics

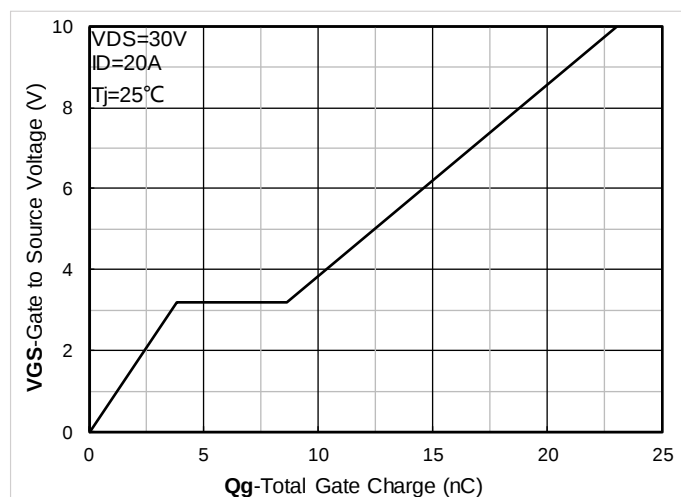


Figure 4. Gate Charge

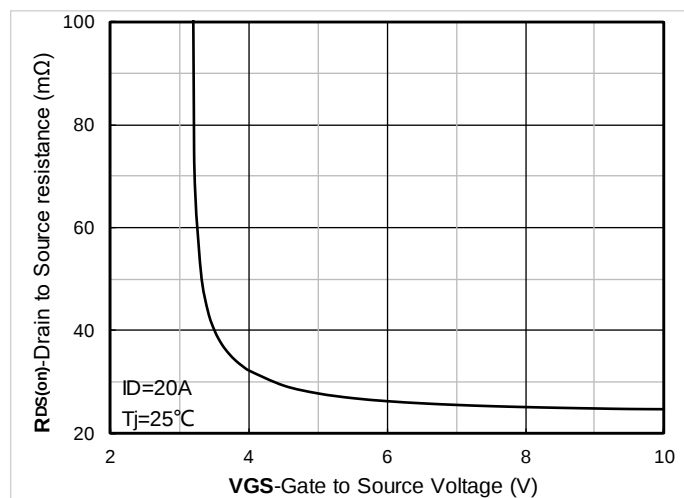


Figure 5. On-Resistance vs Gate to Source Voltage

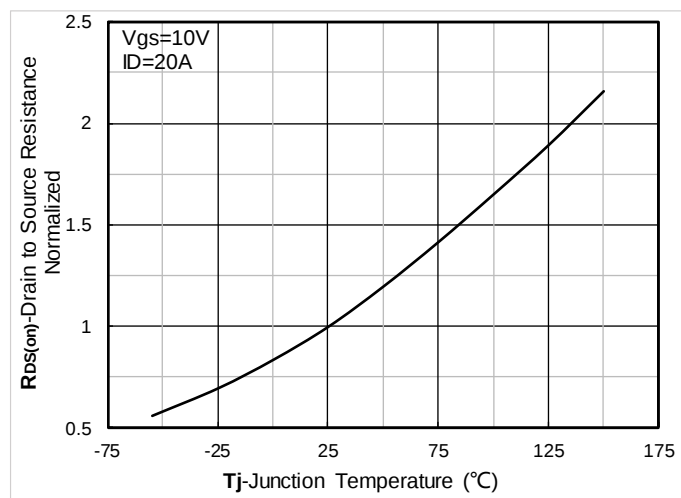


Figure 6. Normalized On-Resistance

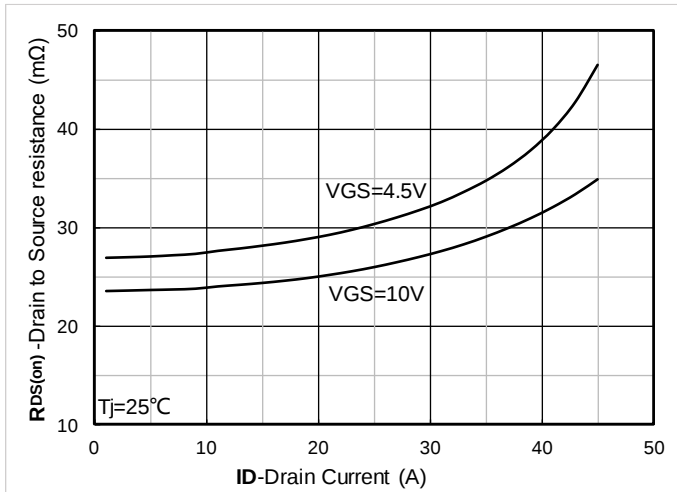


Figure 7. RDS(on) VS Drain Current

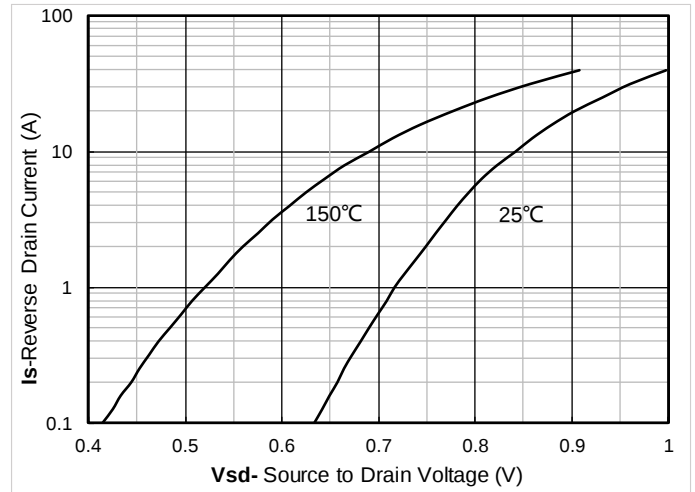


Figure 8. Forward characteristics of reverse diode

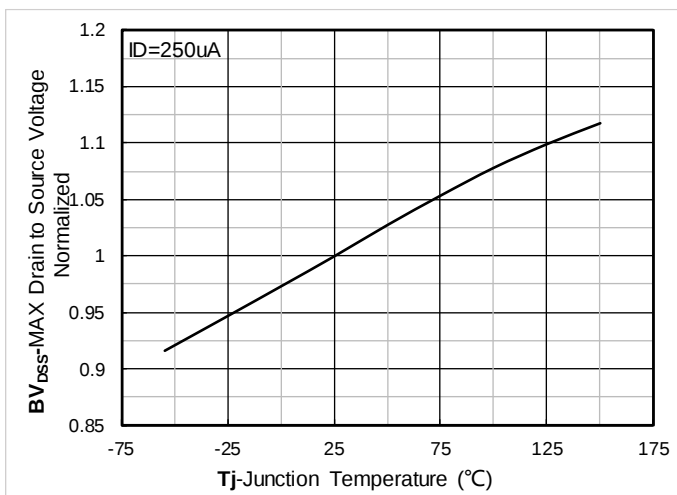


Figure 9. Normalized breakdown voltage

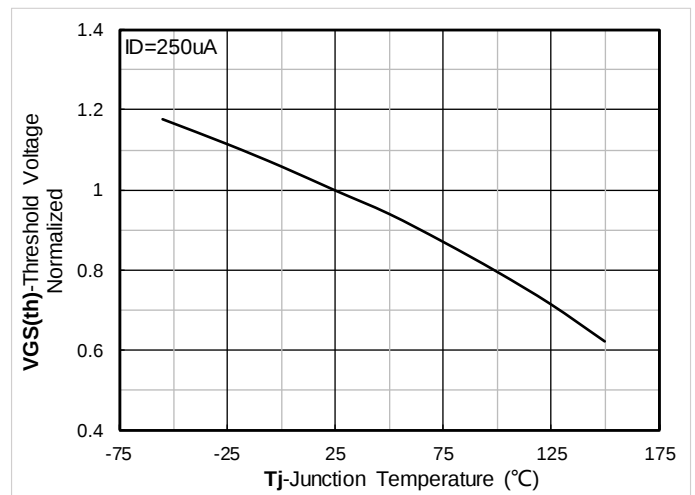
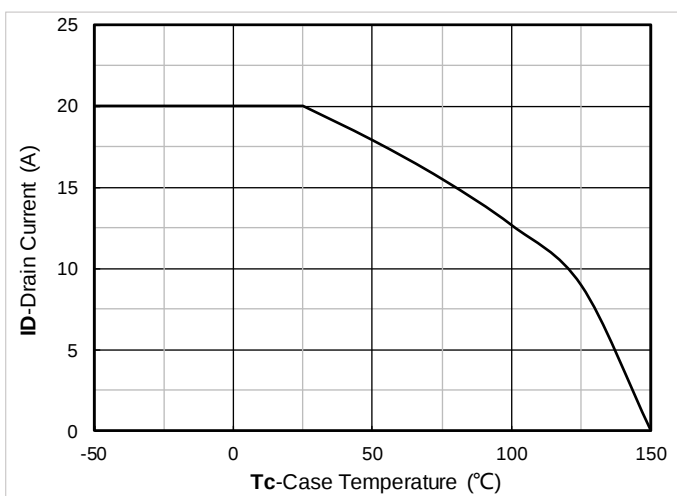


Figure 10. Normalized Threshold voltage



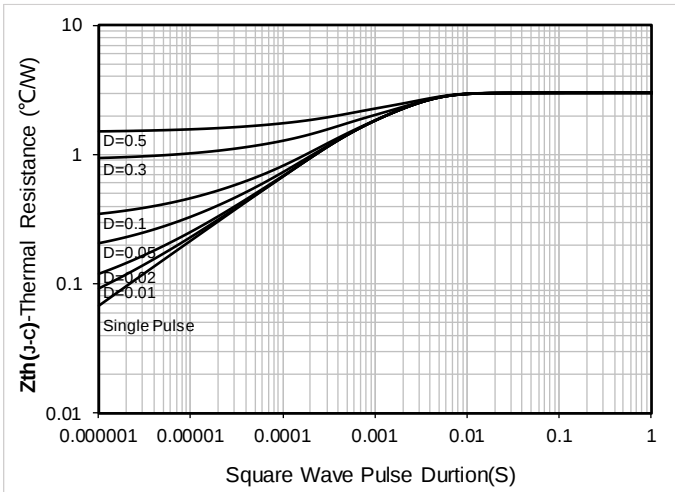


Figure 13. Maximum Transient Thermal Impedance

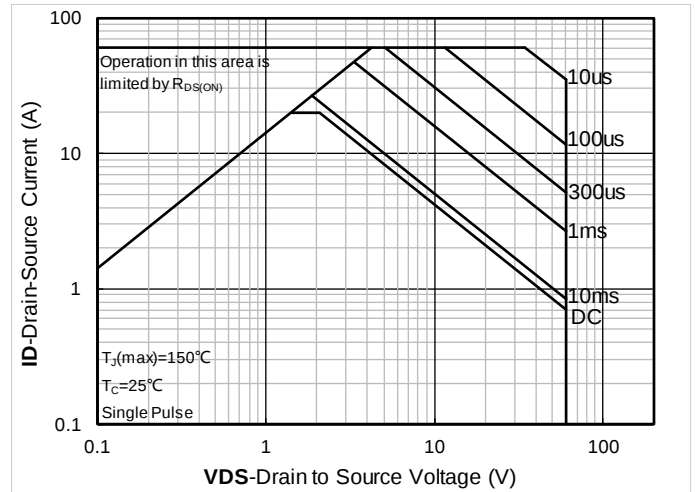


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

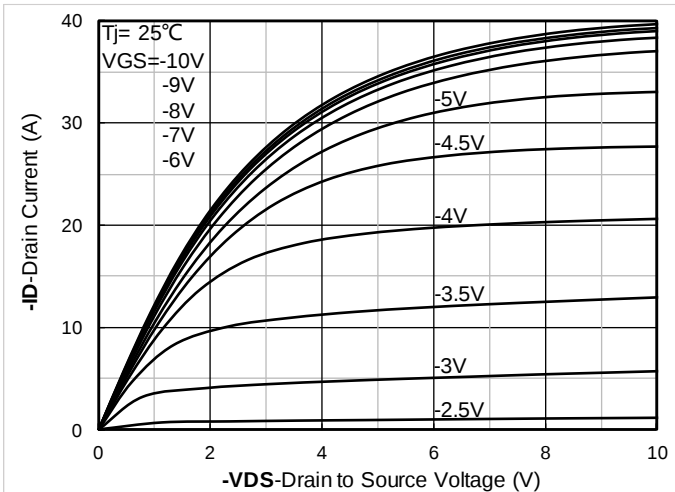


Figure 1. Output Characteristics

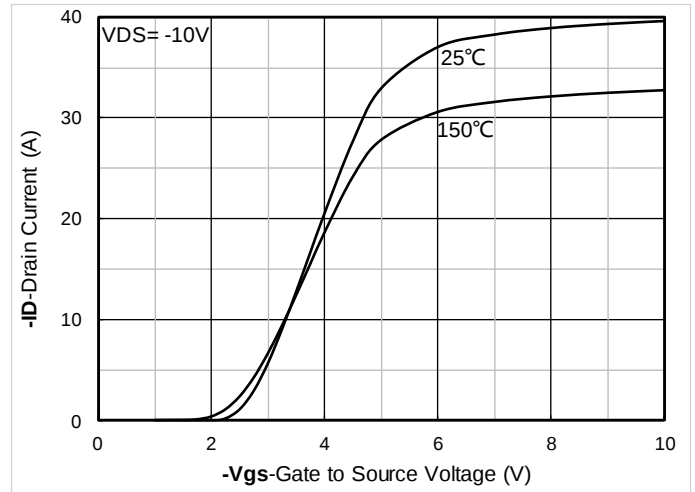


Figure 2. Transfer Characteristics

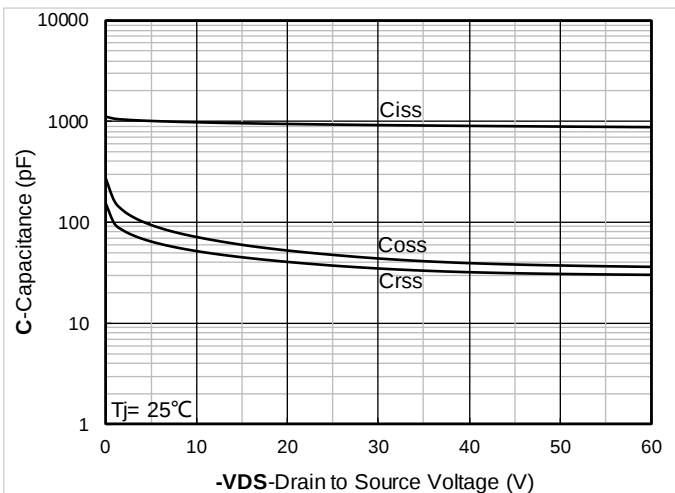


Figure 3. Capacitance Characteristics

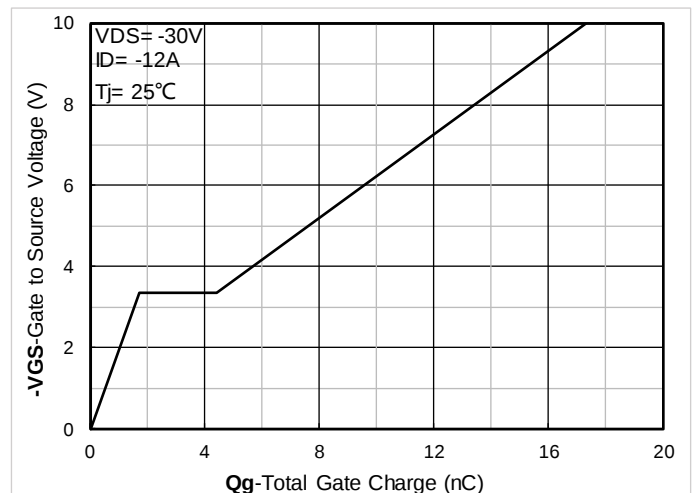


Figure 4. Gate Charge

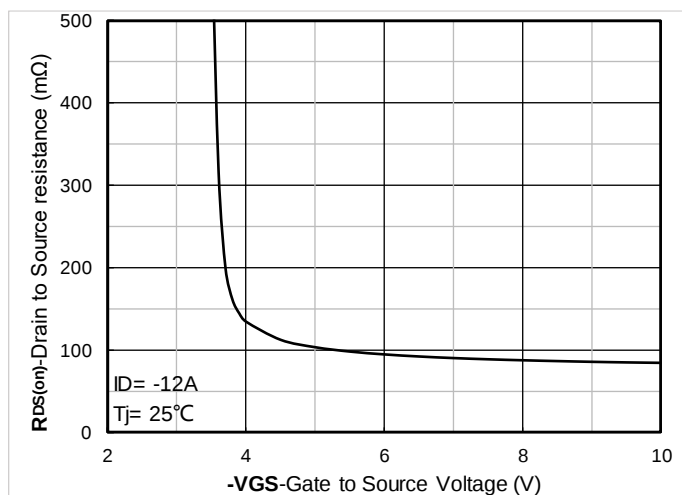


Figure 5. On-Resistance vs Gate to Source Voltage

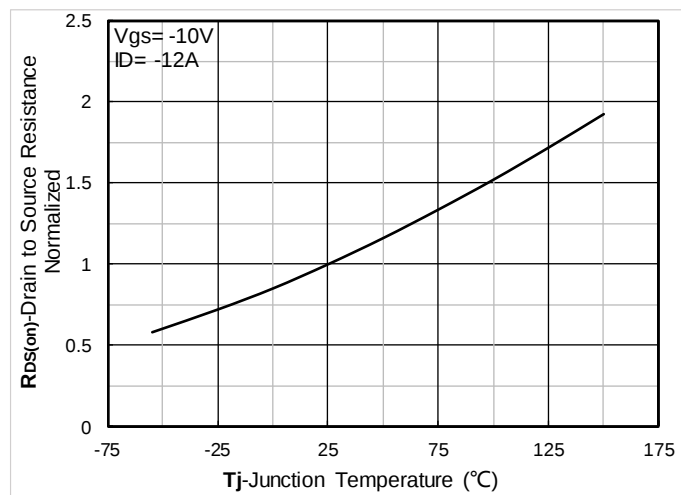


Figure 6. Normalized On-Resistance

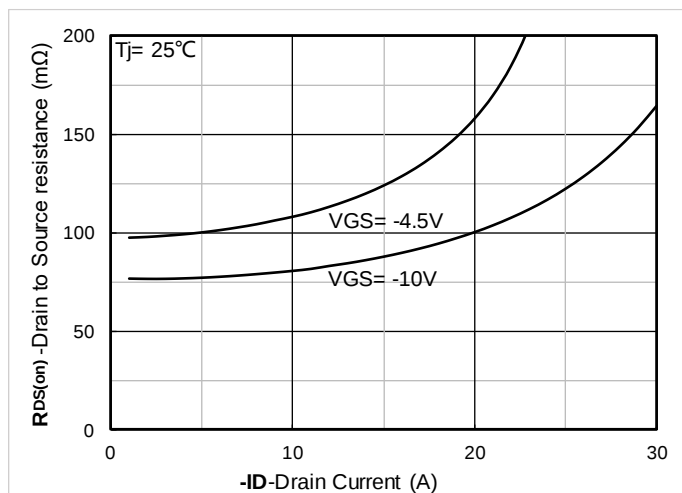


Figure 7. $R_{DS(on)}$ VS Drain Current

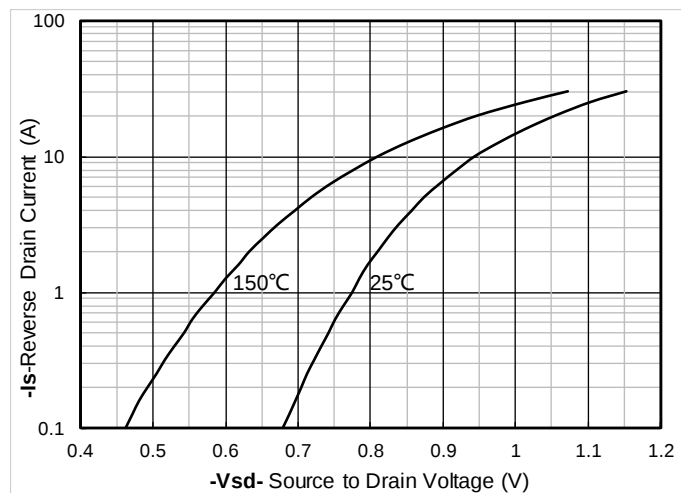


Figure 8. Forward characteristics of reverse diode

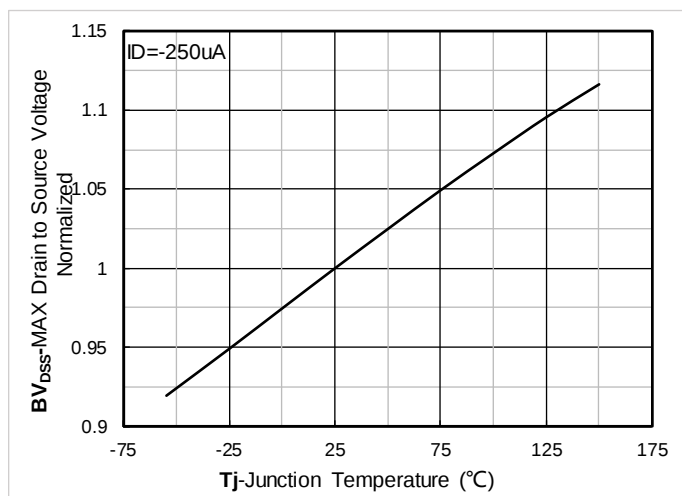


Figure 9. Normalized breakdown voltage

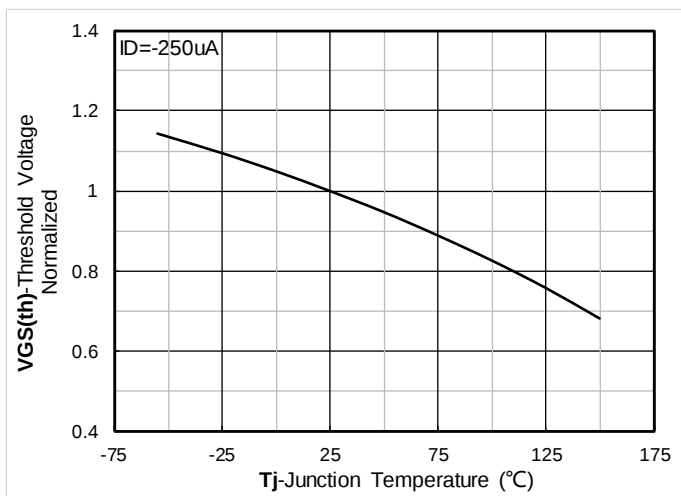


Figure 10. Normalized Threshold voltage

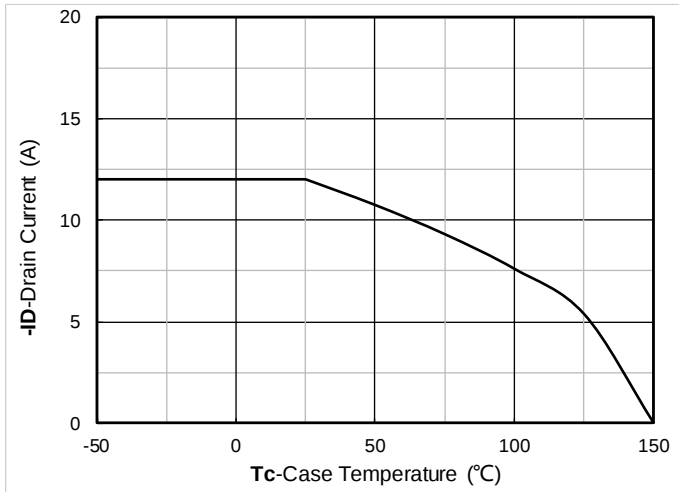


Figure 11. Current dissipation

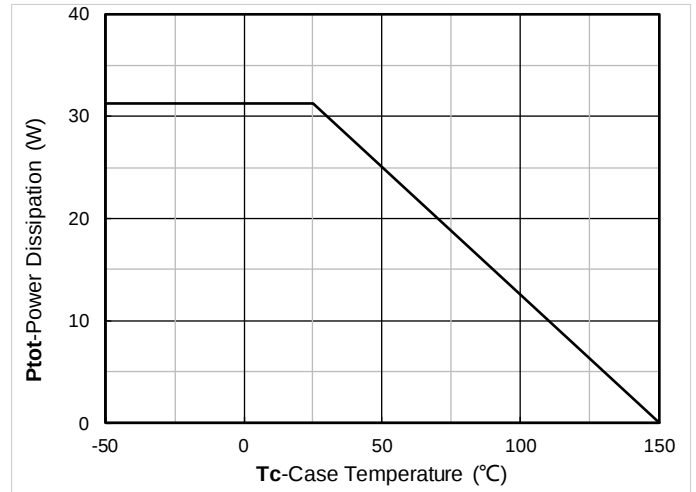
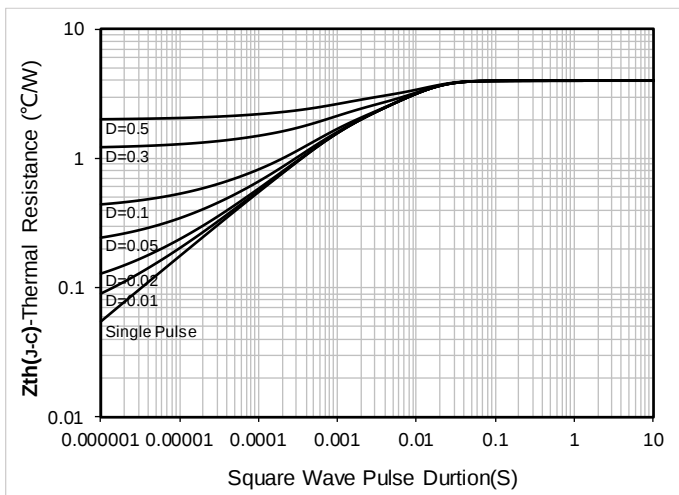
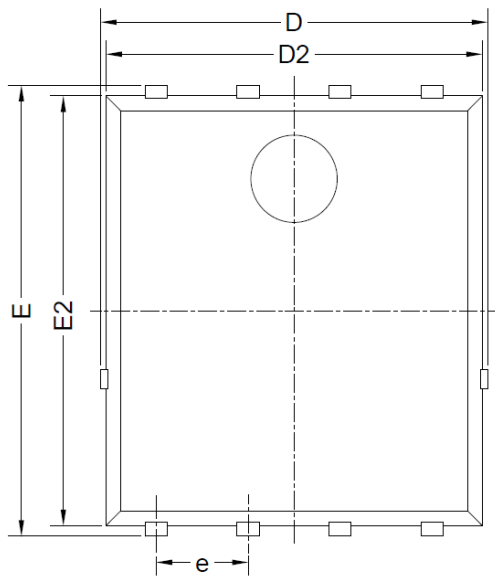


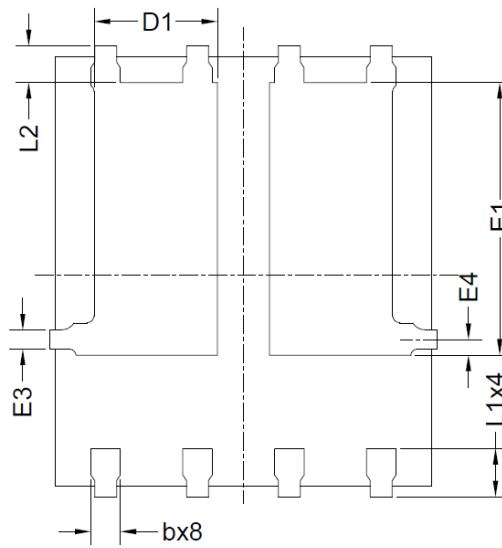
Figure 12. Power dissipation



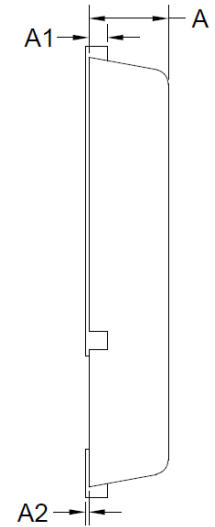
■ PDFN5060-8L-E-1.1MM Package information



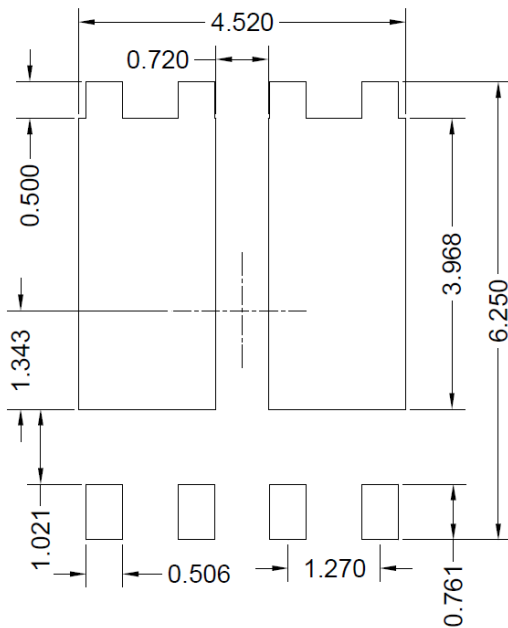
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254REF		
E4	0.21REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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