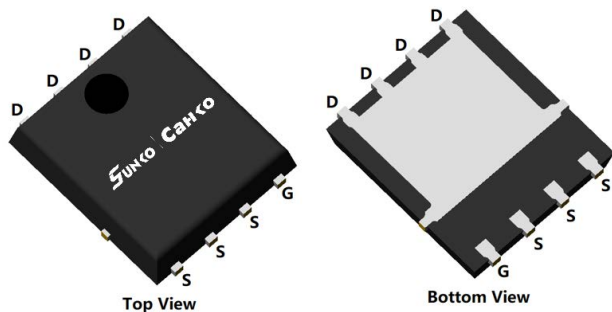
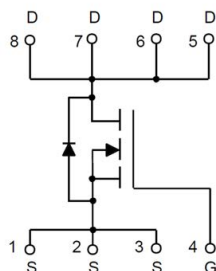


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} 40V
- I_D 80A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<4.4m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<8m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Limiting Values

Parameter			Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	40	V
Gate-source Voltage			V _{GS}	-20	20	V
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C, V _{GS} = 10V	I _D	-	18	A
		T _A =100°C, V _{GS} = 10V		-	12.7	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C, V _{GS} = 10V, Chip limitation		-	80	
		T _C =100°C, V _{GS} = 10V		-	56	
Pulsed Drain Current	T _C =25°C, t _p ≤10μs		I _{DM}	-	320	A
Avalanche energy (non-repetitive)	V _G =10V, R _G =25Ω, L=0.5mH, I _{AS} =15.5A		EAS	-	60	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	2.6	W
		T _A =100°C		-	1.3	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	51	
		T _C =100°C		-	25	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	56	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	2.9	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCG4D4G04A	F1	SCG4D4G04A	5000	10000	100000	13" reel

SCG4D4G04A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	40	-	-	V
		V _{GS} = 0V, I _D =10mA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =32V, V _{GS} =0V	-	-	1	μA
		V _{DS} =32V, V _{GS} =0V, T _j =125°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	3.3	4.4	mΩ
		V _{GS} =4.5V, I _D =20A	-	5.8	8	mΩ
Diode Forward Voltage	V _{SD}	I _S =40A, V _{GS} =0V	-	0.85	1.2	V
Gate resistance	R _G	f=1MHz	-	1.4	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	50	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHz	-	970	-	pF
Output Capacitance	C _{oss}		-	540	-	
Reverse Transfer Capacitance	C _{rss}		-	23	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =50A	-	16.4	-	nC
Gate-Source Charge	Q _{gs}		-	3.3	-	
Gate-Drain Charge	Q _{gd}		-	5	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/us, V _{GS} =0V, V _R =20V	-	7	-	nC
Reverse Recovery Time	t _{rr}		-	19.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =20V, I _D =50A, R _L =0.4Ω R _{GEN} =3Ω	-	8.4	-	ns
Turn-on Rise Time	t _r		-	11.9	-	
Turn-off Delay Time	t _{D(off)}		-	18.7	-	
Turn-off fall Time	t _f		-	5.8	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

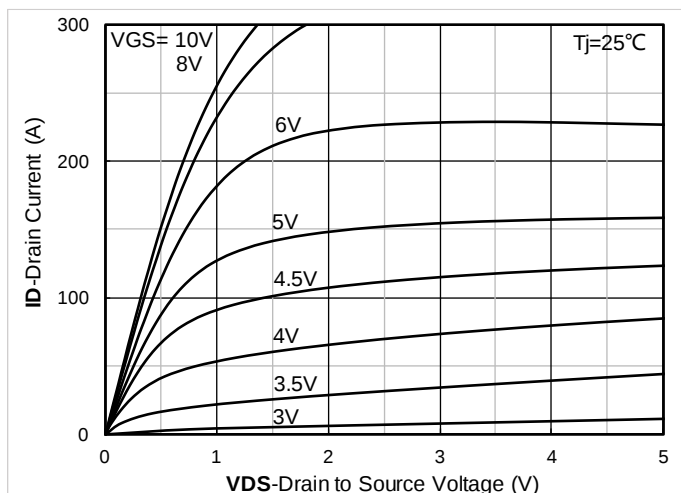


Figure 1. Output Characteristics

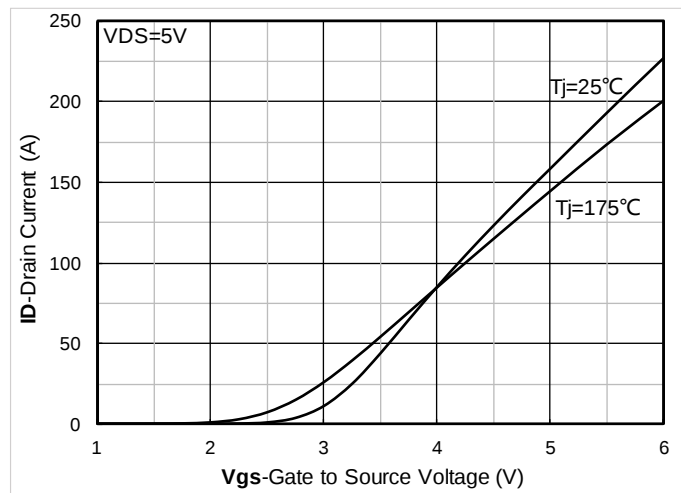


Figure 2. Transfer Characteristics

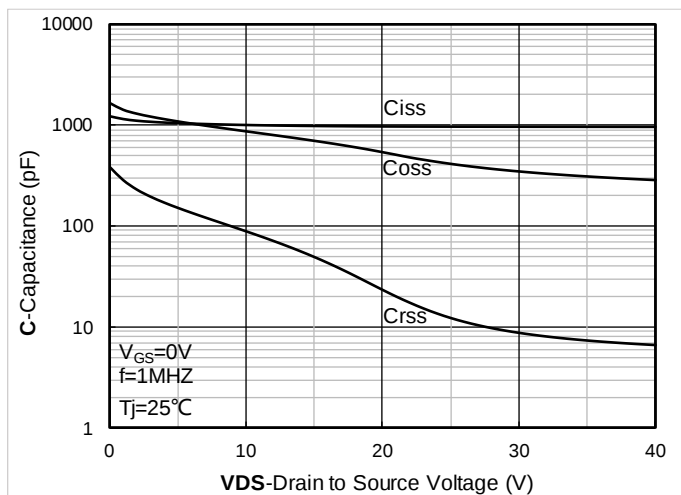


Figure 3. Capacitance Characteristics

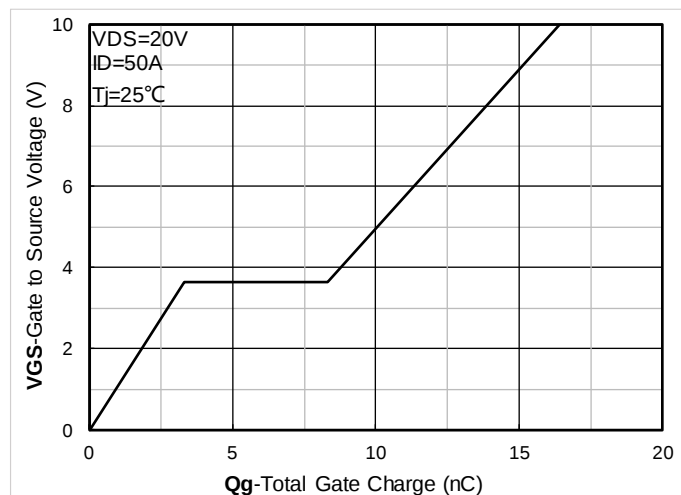


Figure 4. Gate Charge

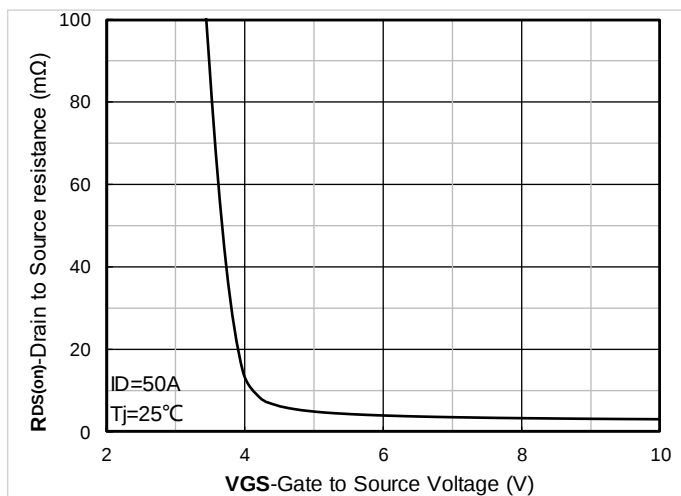


Figure 5. On-Resistance vs Gate to Source Voltage

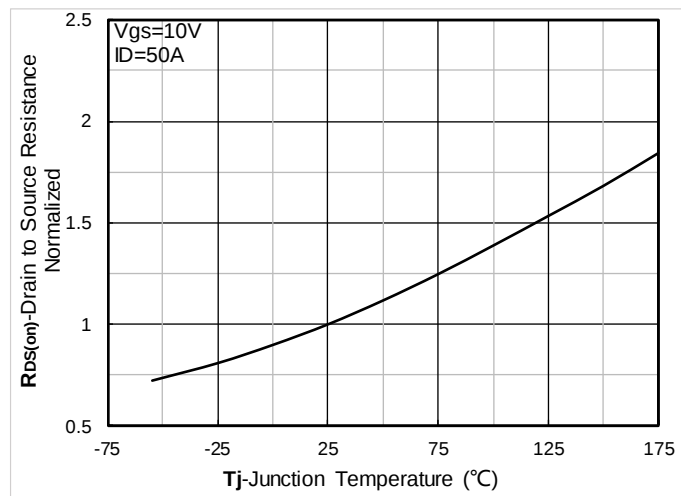


Figure 6. Normalized On-Resistance

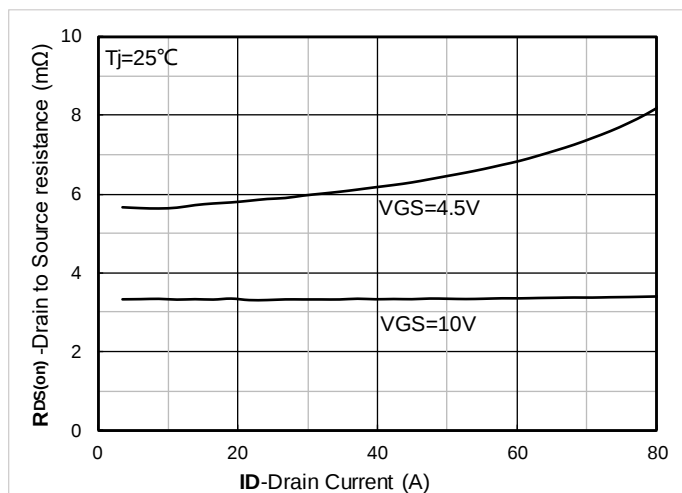


Figure 7. $R_{DS(on)}$ VS Drain Current

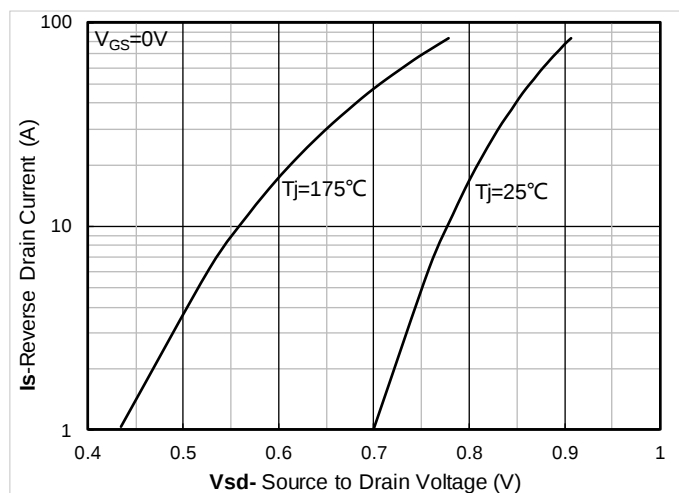


Figure 8. Forward characteristics of reverse diode

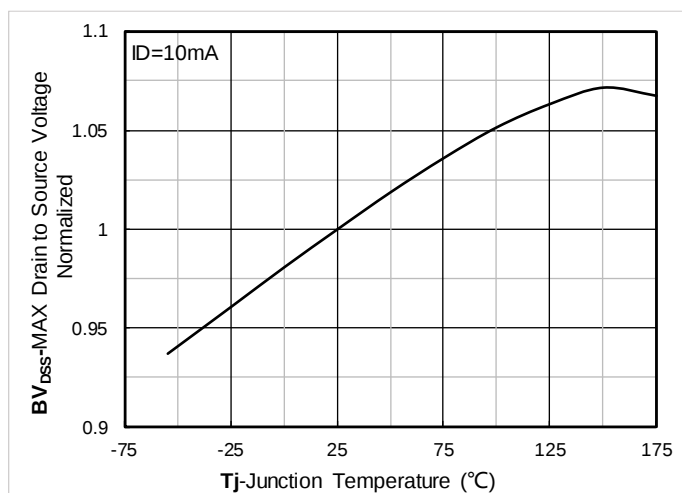


Figure 9. Normalized breakdown voltage

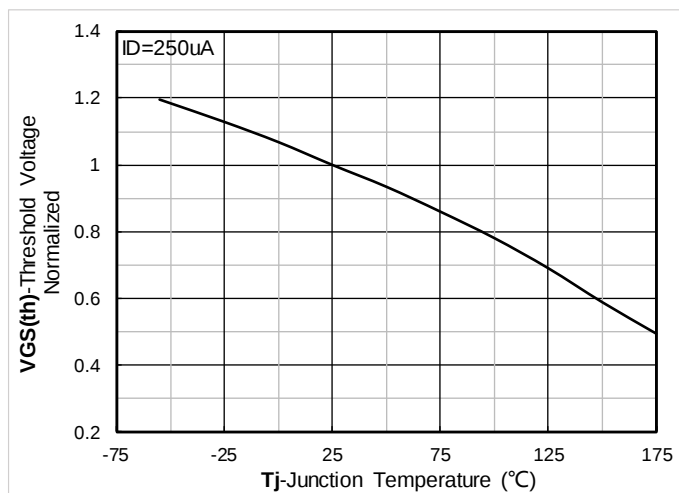


Figure 10. Normalized Threshold voltage

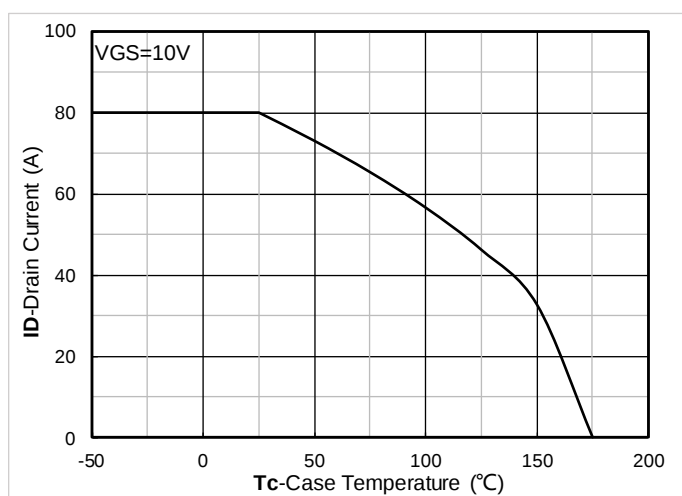


Figure 11. Current dissipation

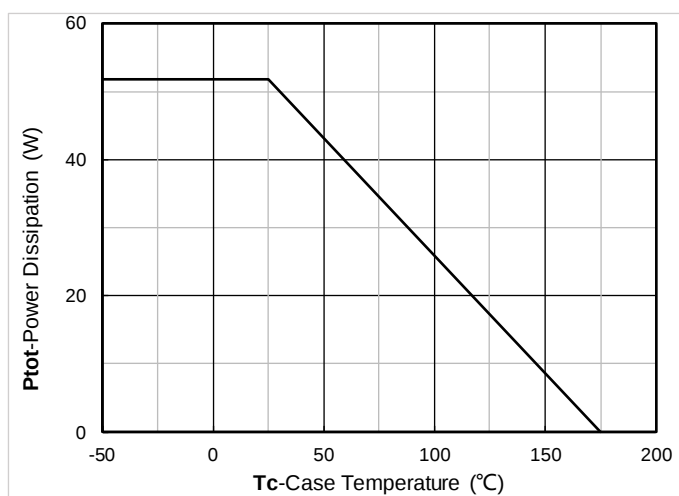


Figure 12. Power dissipation

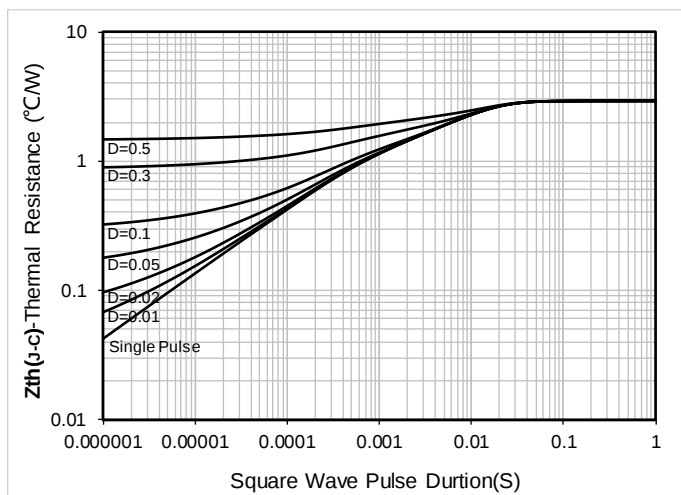


Figure 13. Maximum Transient Thermal Impedance

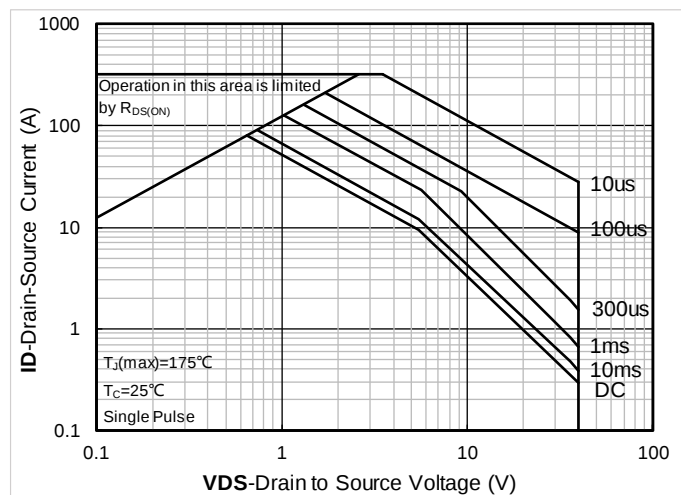


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

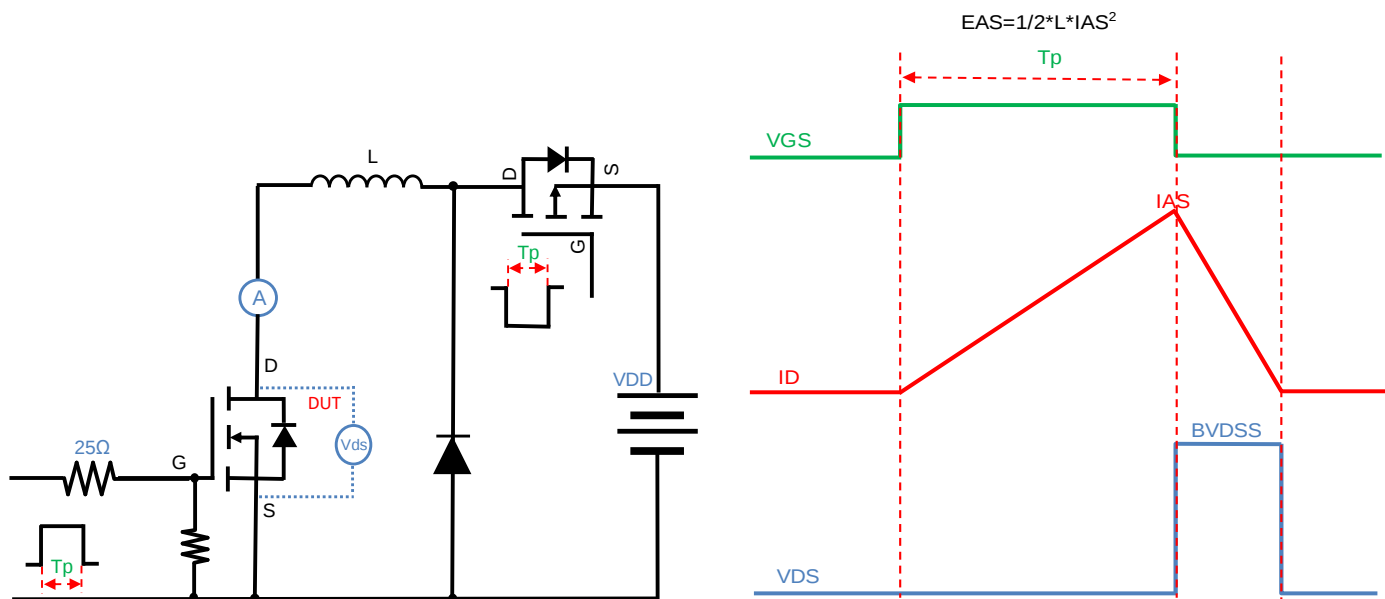


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform



Figure C. Resistive Switching Test Circuit & Waveform

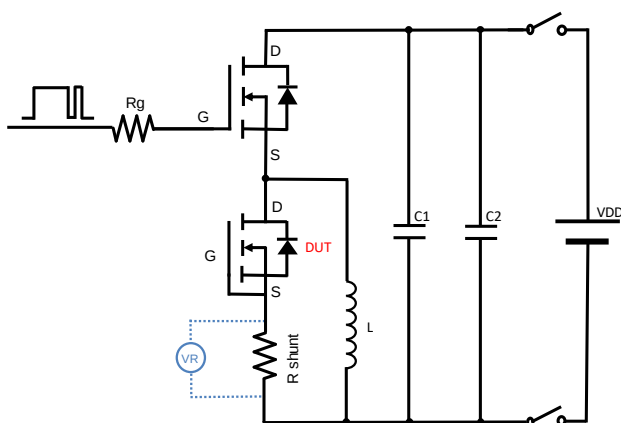
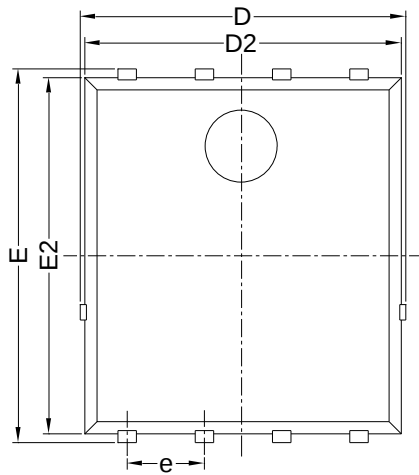
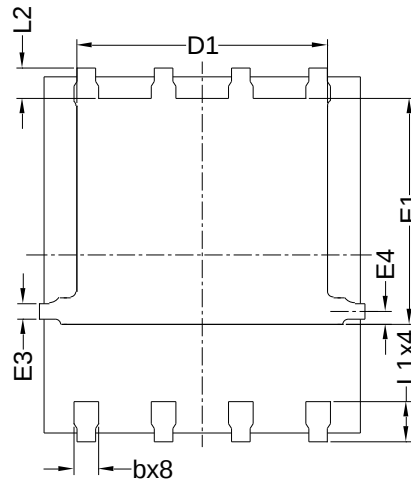


Figure D. Diode Recovery Test Circuit & Waveform

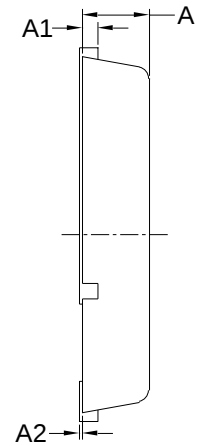
■ PDFN5060-8L-B-1.1mm Package information



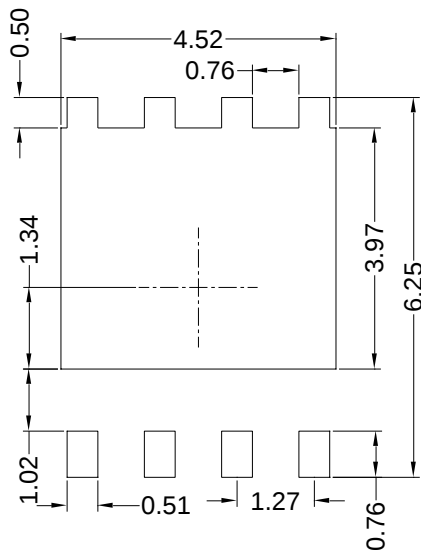
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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