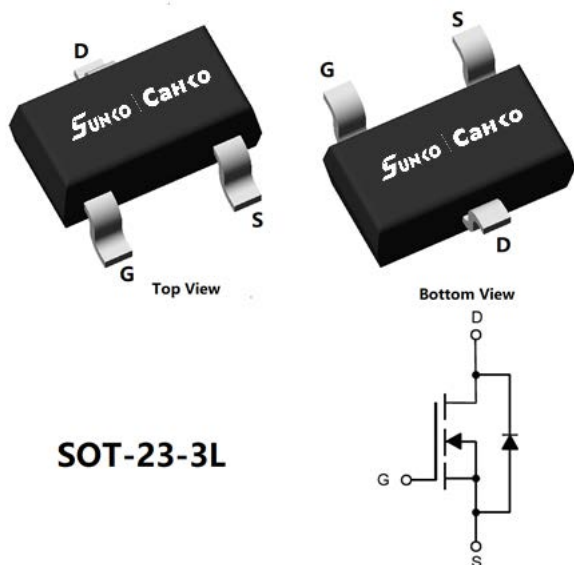


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	100V
• I_D	2.1A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<100m Ω
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<110m Ω

General Description

- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- PWM applications
- Power management
- Load switch

Limiting Values

Parameter	Conditions	Symbol	Min	Max	Unit
Drain-source Voltage	$T_J \geq 25^\circ\text{C}; T_J \leq 150^\circ\text{C}$	V_{DS}	-	100	V
Gate-source Voltage	$T_J \leq 150^\circ\text{C}; \text{DC}$	V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	I_D	-	2.1	A
	$T_A = 25^\circ\text{C}, V_{GS} = 10V$		-	1.3	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p \leq 10\mu\text{s}$	I_{DM}	-	16.8	
Maximum Body-Diode Continuous Current	$T_A = 25^\circ\text{C}$	I_S	-	1.1	W
Total Power Dissipation (Note 1,2)	Steady-State	P_D	-	1.0	
	$T_A = 100^\circ\text{C}$		-	0.4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55	150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	-	126	$^\circ\text{C/W}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCL100N10AL	F2	100AL.	3000	30000	120000	7" reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _j =25℃	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _j =25℃	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =150℃	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25℃	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _j =25℃	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2A, T _j =25℃	-	77	100	mΩ
		V _{GS} =4.5V, I _D =1A, T _j =25℃	-	84	110	mΩ
Diode Forward Voltage	V _{SD}	I _S =2A, V _{GS} =0V, T _j =25℃	-	0.77	1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25℃	-	1.7	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz, T _j =25℃	-	903	-	pF
Output Capacitance	C _{oss}		-	30	-	
Reverse Transfer Capacitance	C _{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =2A, T _j =25℃	-	23.2	-	nC
Gate-Source Charge	Q _{gs}		-	2.6	-	
Gate-Drain Charge	Q _{gd}		-	6.1	-	
Reverse Recovery Charge	Q _{rr}	I _F =2A, di/dt=100A/μs, V _{GS} =0V, V _R =50V, T _j =25℃	-	25	-	nC
Reverse Recovery Time	t _{rr}		-	22	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =50V, I _D =2A, R _L =25Ω, R _{GEN} =3Ω, T _j =25℃	-	7.4	-	ns
Turn-on Rise Time	t _r		-	3.4	-	
Turn-off Delay Time	t _{D(off)}		-	28.6	-	
Turn-off Fall Time	t _f		-	4.3	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

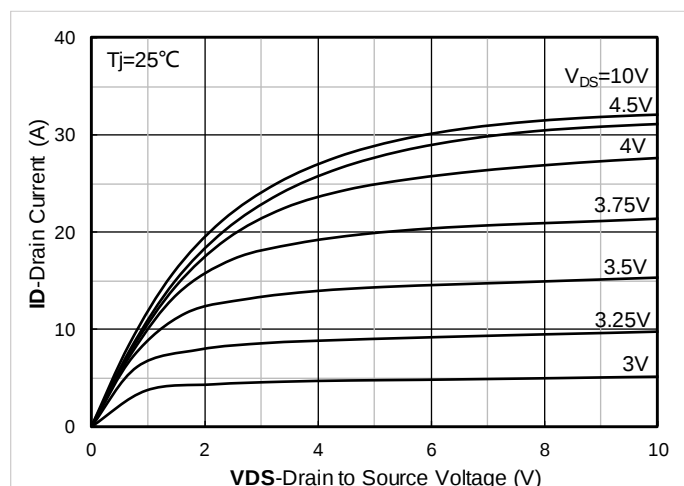


Figure 1. Output Characteristics; typical values

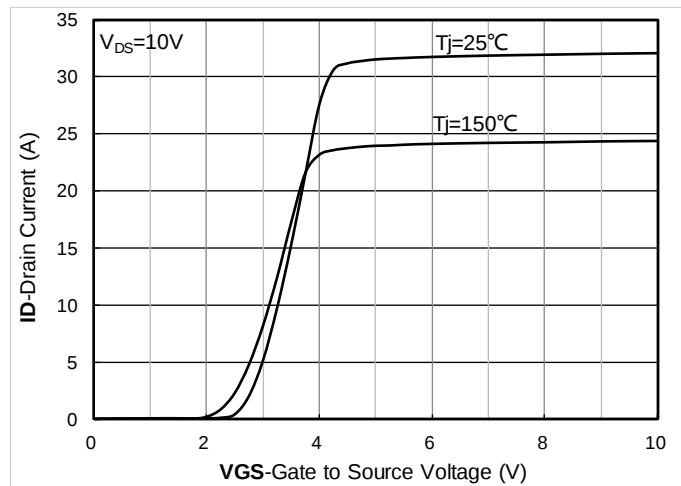


Figure 2. Transfer Characteristics; typical values

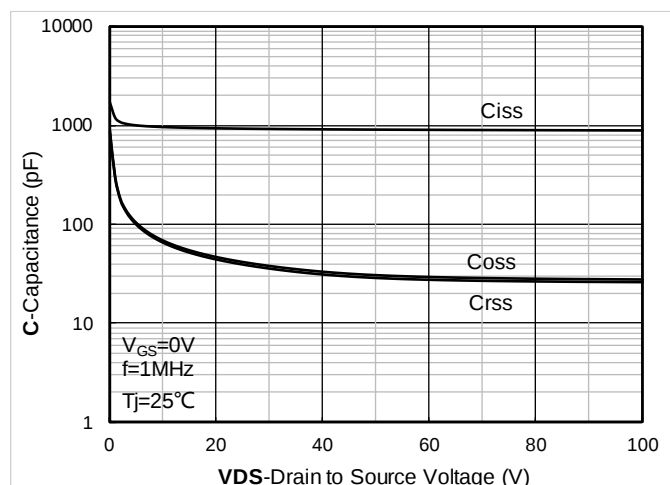


Figure 3. Capacitance Characteristics; typical values

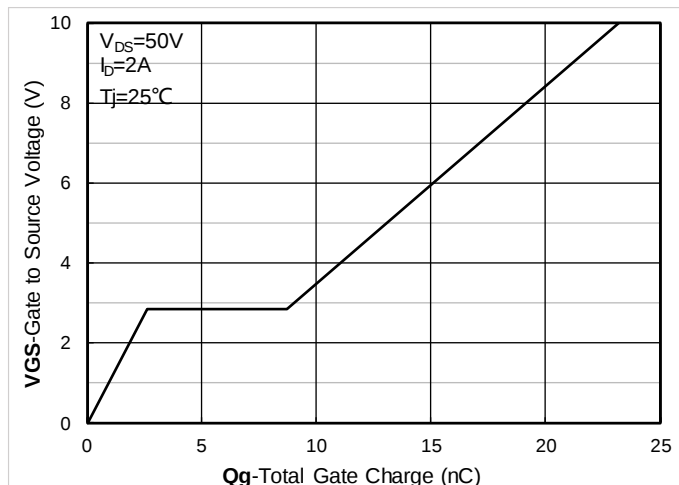


Figure 4. Gate Charge; typical values

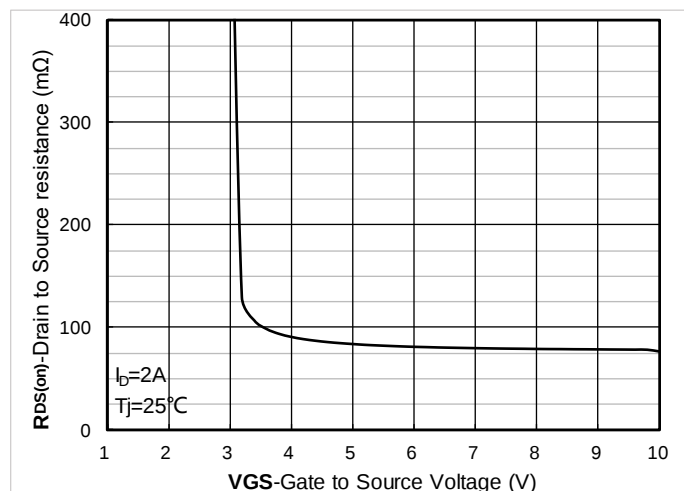


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

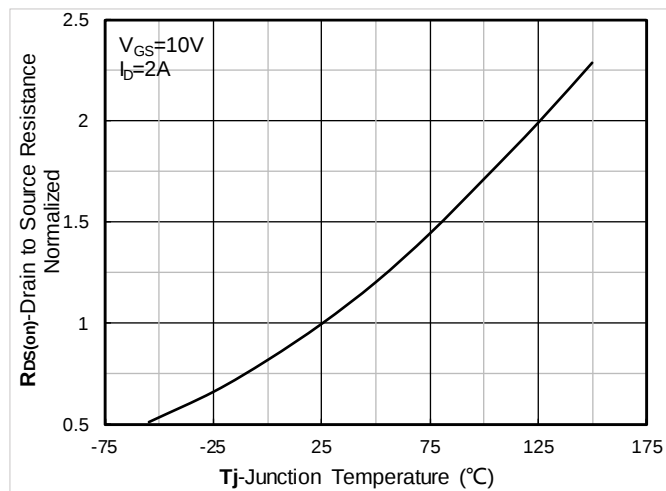


Figure 6. Normalized On-Resistance

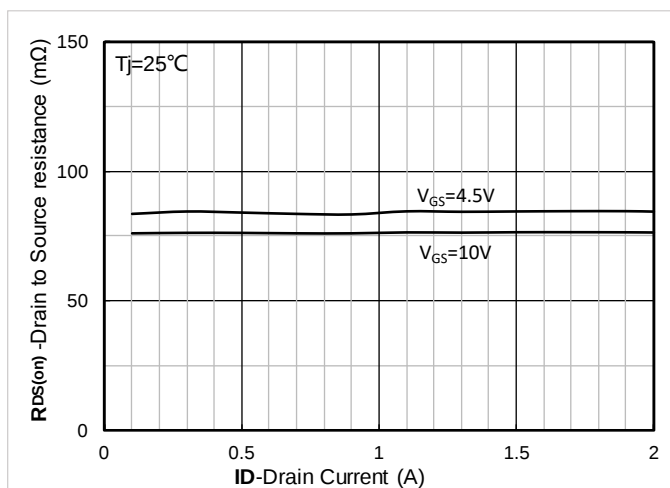


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

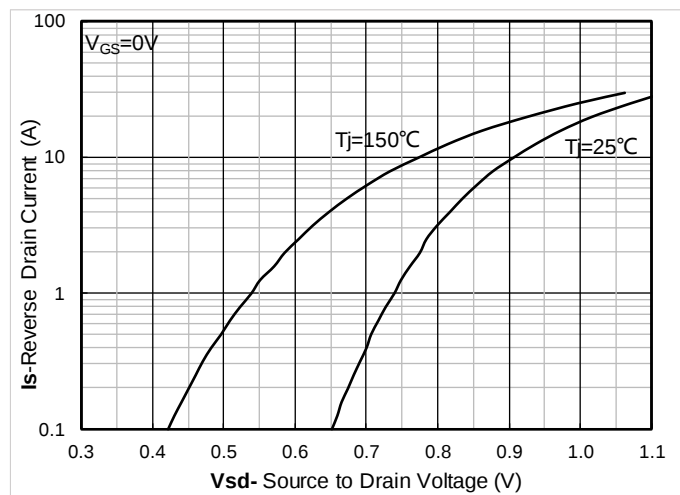


Figure 8. Forward characteristics of reverse diode; typical values

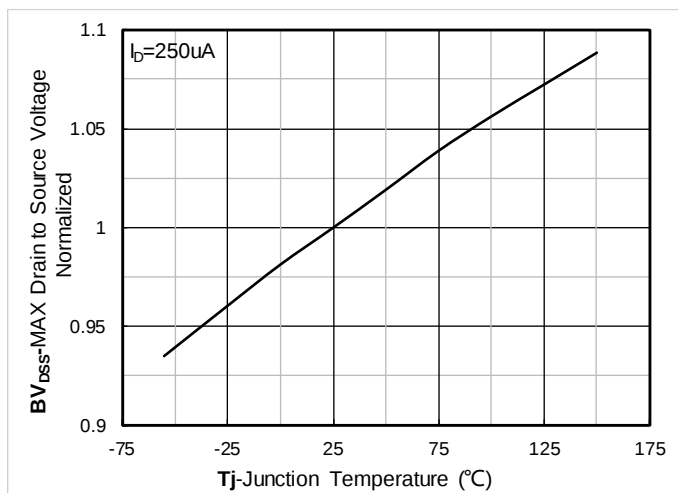


Figure 9. Normalized breakdown voltage

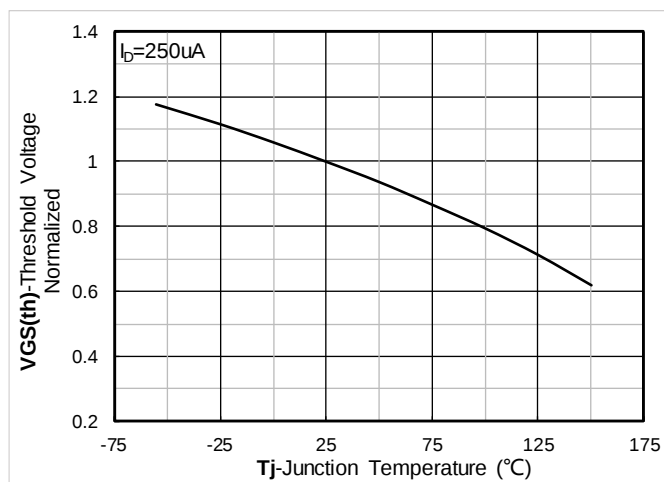


Figure 10. Normalized Threshold voltage

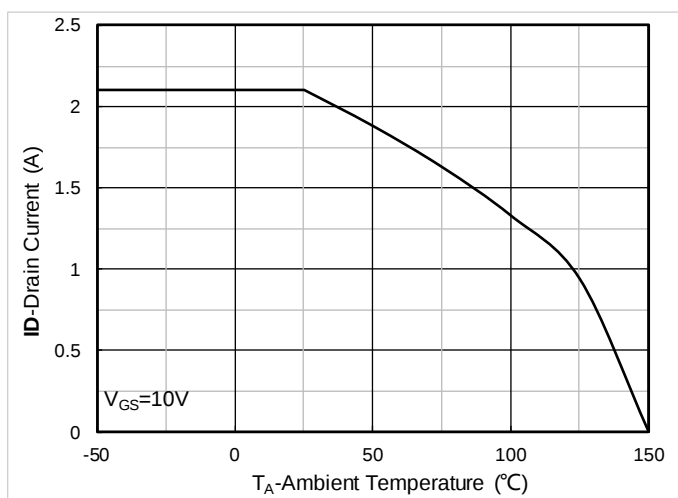


Figure 11. Current dissipation

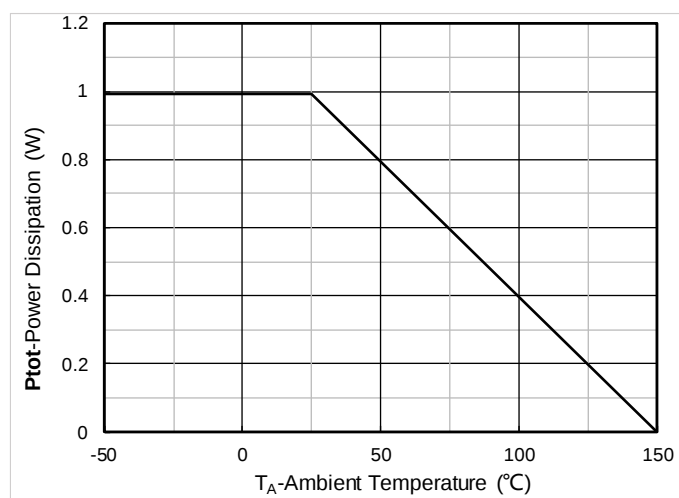


Figure 12. Power dissipation

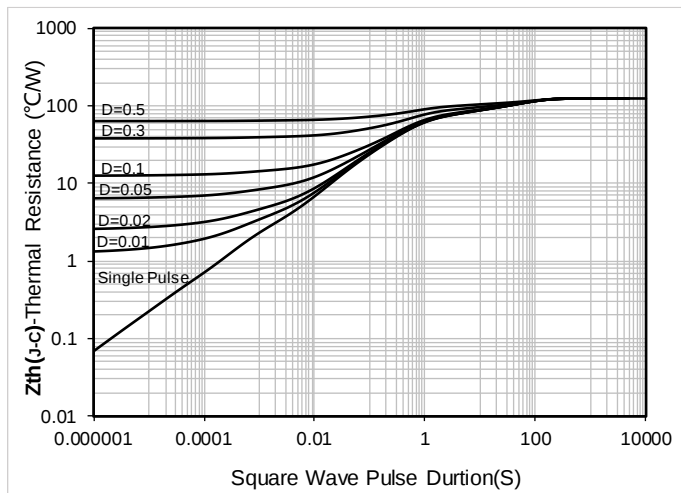


Figure 13. Maximum Transient Thermal Impedance

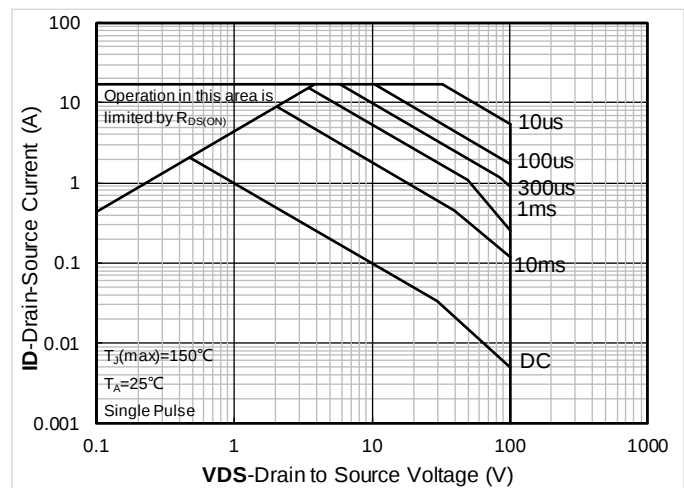
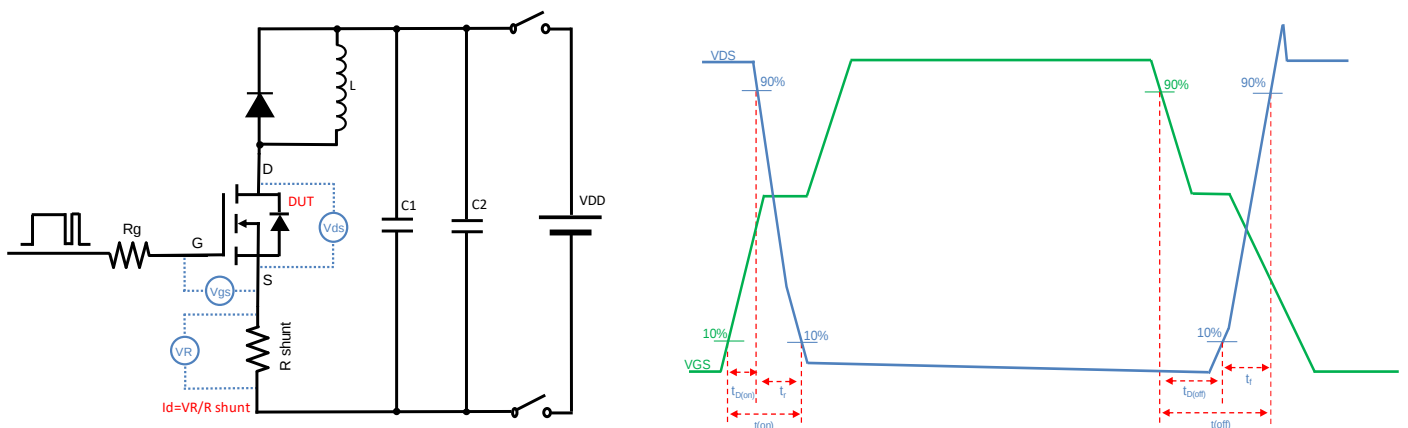
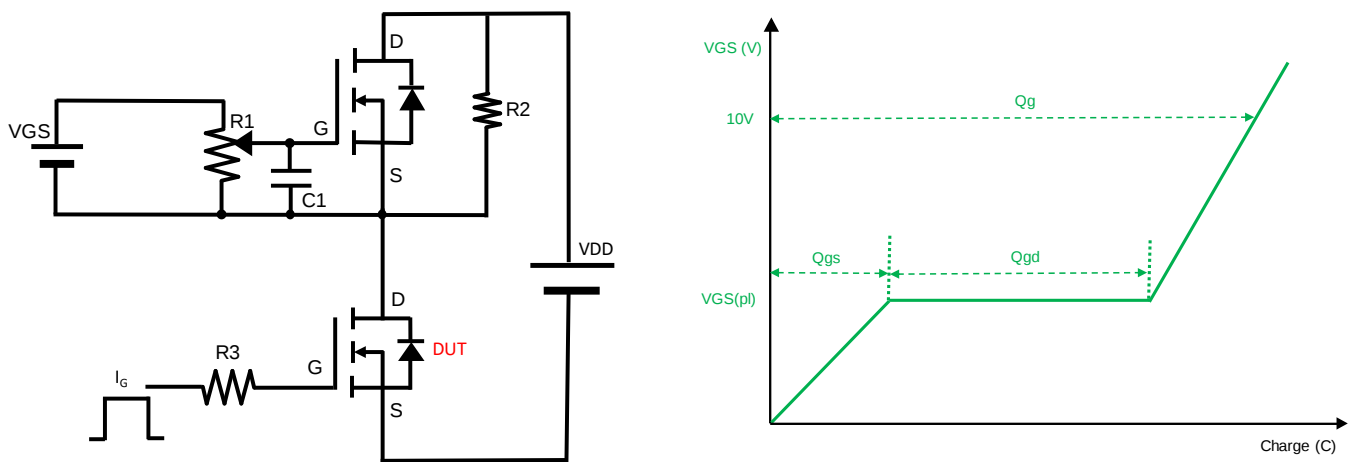
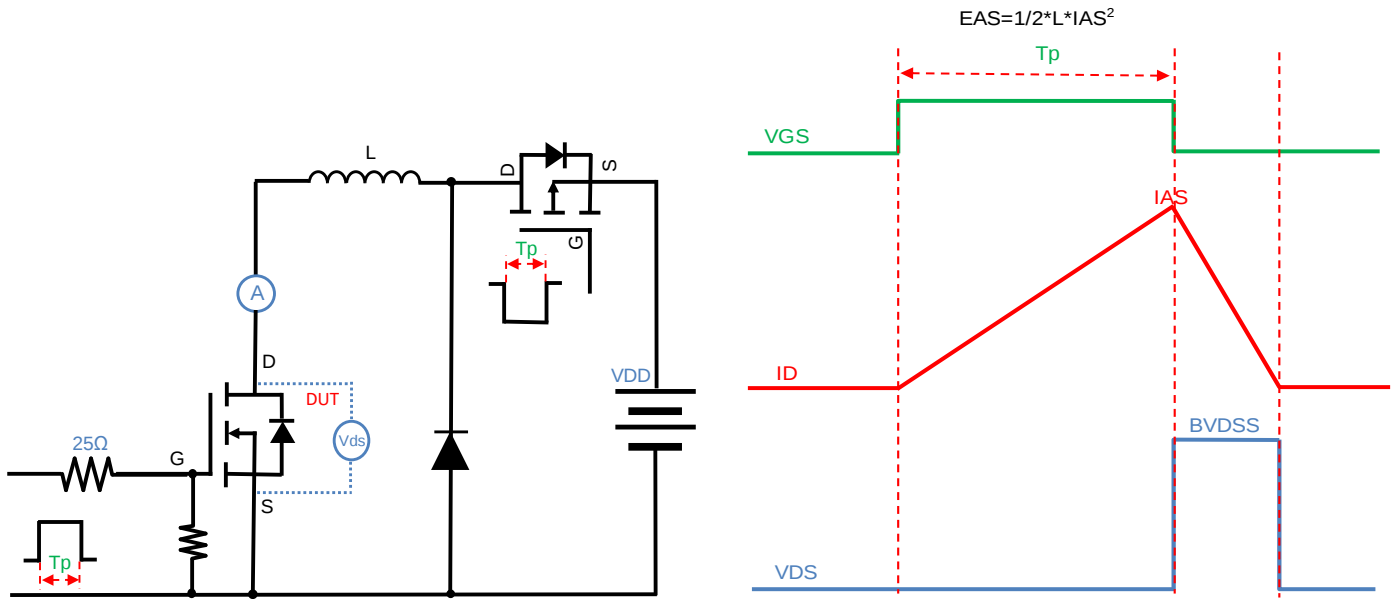


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms



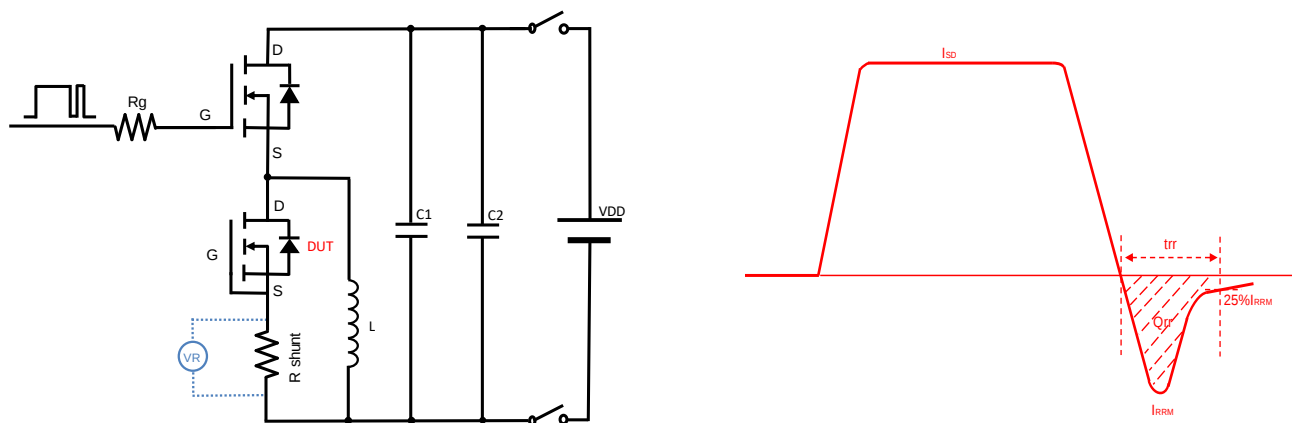
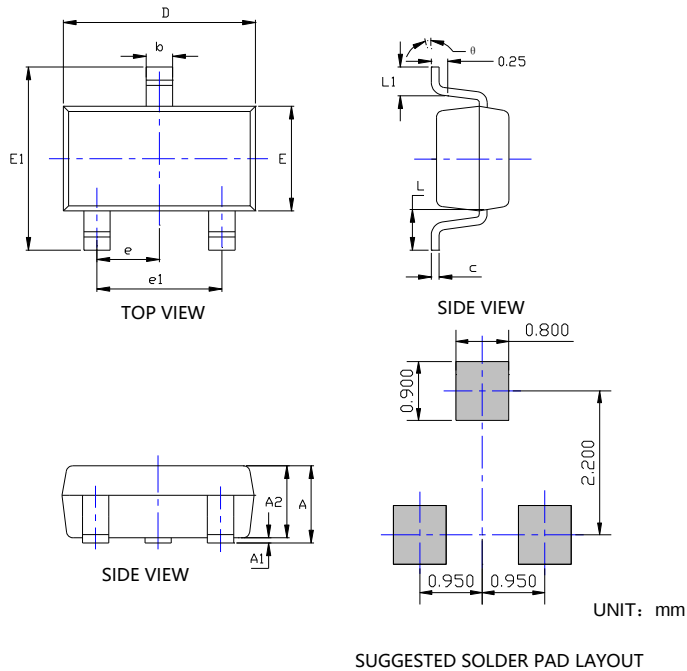


Figure D. Diode Recovery Test Circuit & Waveform

■ SOT-23-3L Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.041	---	0.049	1.050	---	1.250
A1	0.000	---	0.008	0.000	---	0.200
A2	0.041	0.043	0.045	1.050	1.100	1.150
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.111	0.115	0.119	2.820	2.920	3.020
E	0.059	0.063	0.067	1.500	1.600	1.700
E1	0.104	0.110	0.116	2.650	2.800	2.950
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.024REF			0.600REF		
L1	0.012	0.018	0.024	0.300	0.450	0.600
θ	0°	---	8°	0°	---	8°

NOTE:
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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