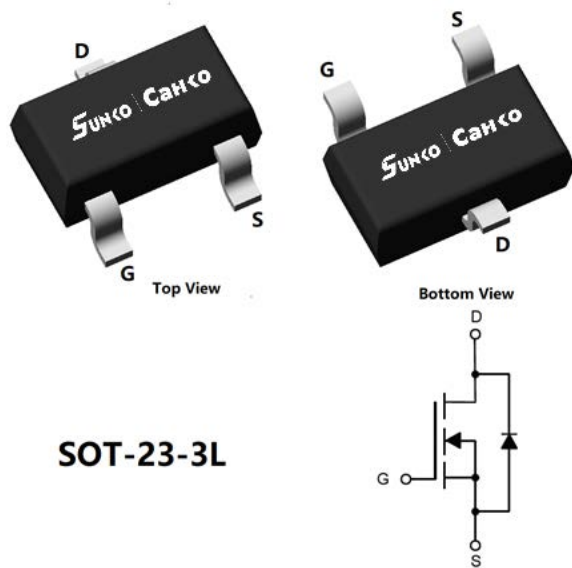


SCL140G10ALJ

N-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	100V
• I_D	1.8A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<140m Ω
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<180m Ω

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC convertor
- Power management functions

■ Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V _{DS}	100	V
Gate-source Voltage			V _{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C, V _{GS} = 10V	I _D	1.8	A
		T _A =100°C, V _{GS} = 10V		1.1	
Pulsed Drain Current	T _C =25°C, t _p =100μs		I _{DM}	15	A
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	0.96	W
		T _A =100°C		0.38	
Junction and Storage Temperature Range			T _J , T _{STG}	-55~+150	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	105	130	$^\circ\text{C/W}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCL140G10ALJ	F2	140G10.	3000	30000	120000	7" reel

SCL140G10ALJ

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1.8A	-	115	140	mΩ
		V _{GS} =4.5V, I _D =1A	-	133	180	mΩ
Diode Forward Voltage	V _{SD}	I _S =1.8A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	21.5	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	1.8	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	134	-	pF
Output Capacitance	C _{oss}		-	30	-	
Reverse Transfer Capacitance	C _{rss}		-	2.7	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =1.8A	-	2.4	-	nC
Gate-Source Charge	Q _{gs}		-	0.15	-	
Gate-Drain Charge	Q _{gd}		-	0.55	-	
Reverse Recovery Charge	Q _{rr}	I _F =1.8A, di/dt=100A/us	-	28.7	-	nC
Reverse Recovery Time	t _{rr}		-	45.4	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =1.8A R _{GEN} =3Ω	-	3.5	-	ns
Turn-on Rise Time	t _r		-	14.9	-	
Turn-off Delay Time	t _{D(off)}		-	13.2	-	
Turn-off fall Time	t _f		-	20.8	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

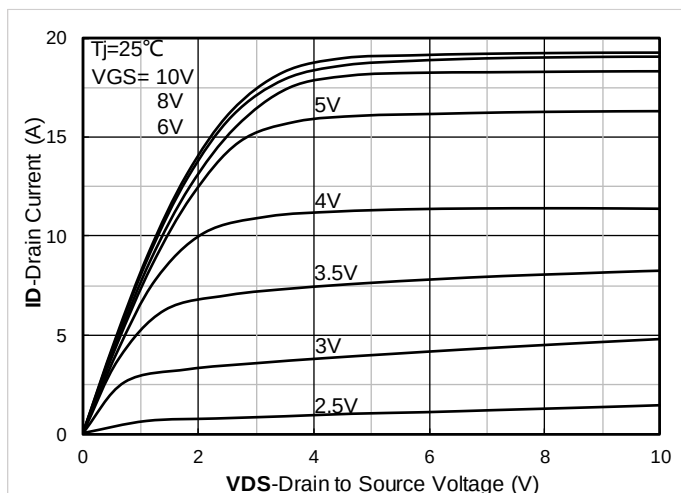


Figure 1. Output Characteristics

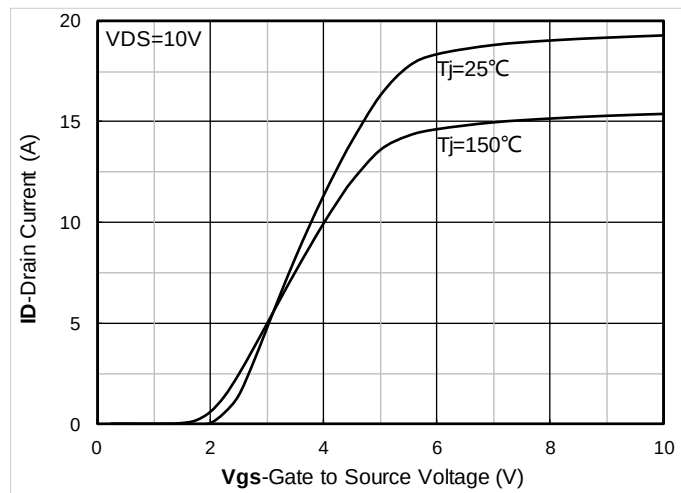


Figure 2. Transfer Characteristics

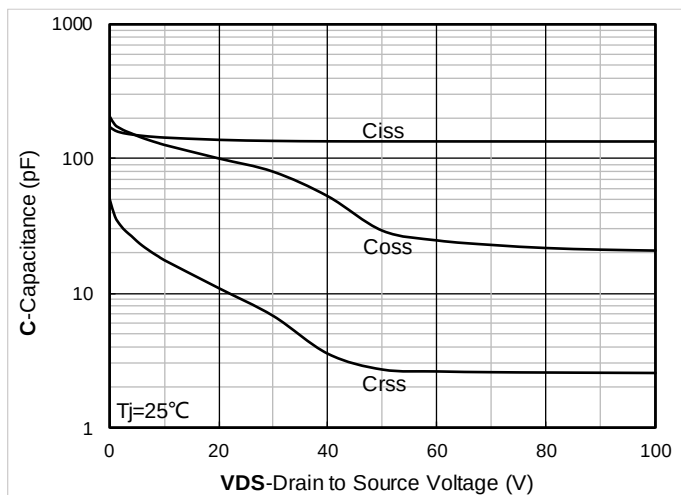


Figure 3. Capacitance Characteristics

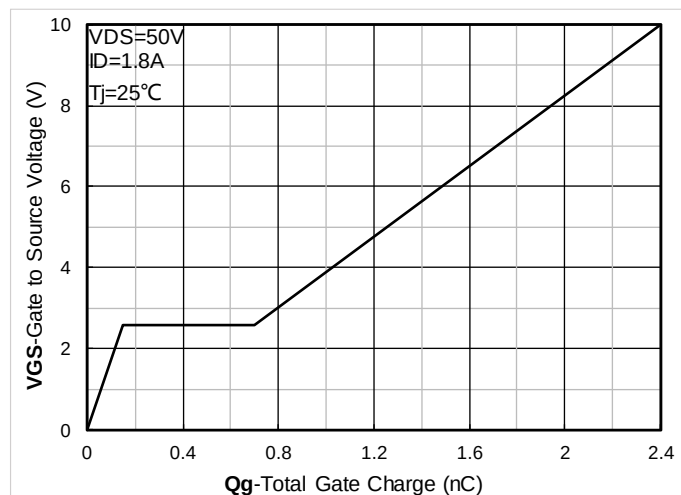


Figure 4. Gate Charge

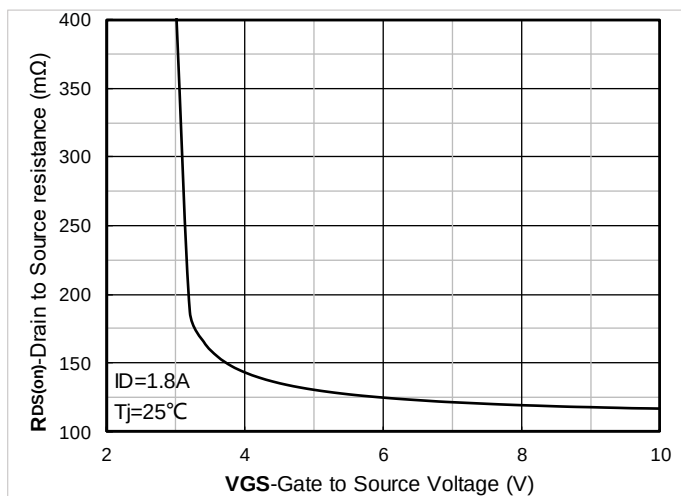


Figure 5. On-Resistance vs Gate to Source Voltage

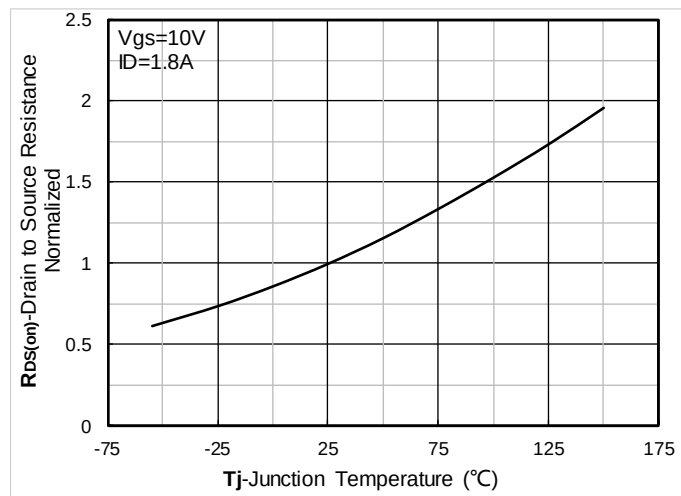


Figure 6. Normalized On-Resistance

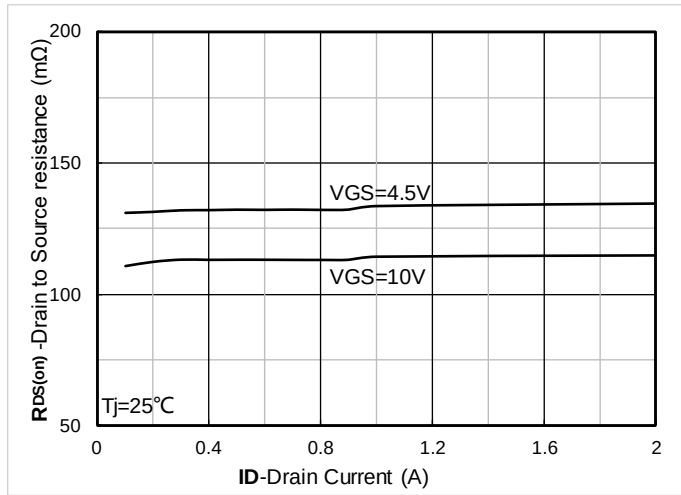


Figure 7. RDS(on) VS Drain Current

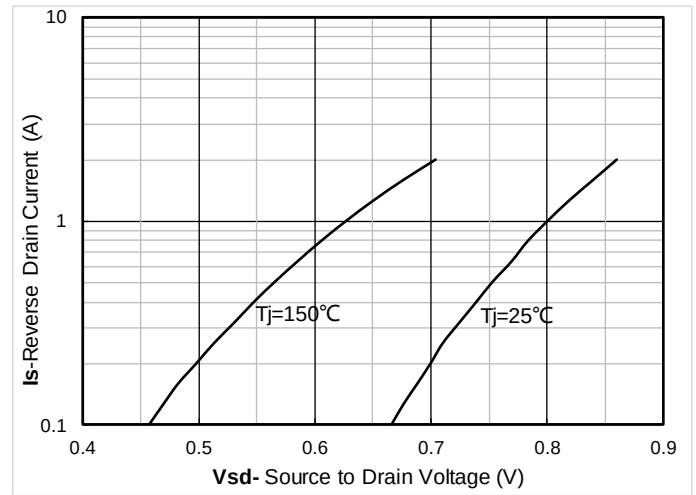


Figure 8. Forward characteristics of reverse diode

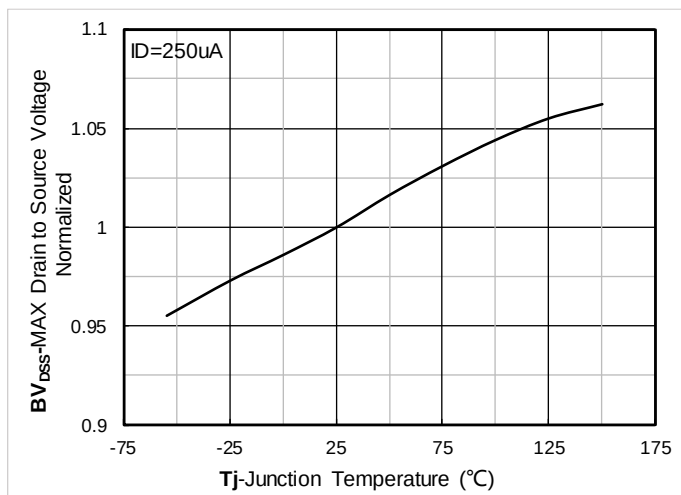


Figure 9. Normalized breakdown voltage

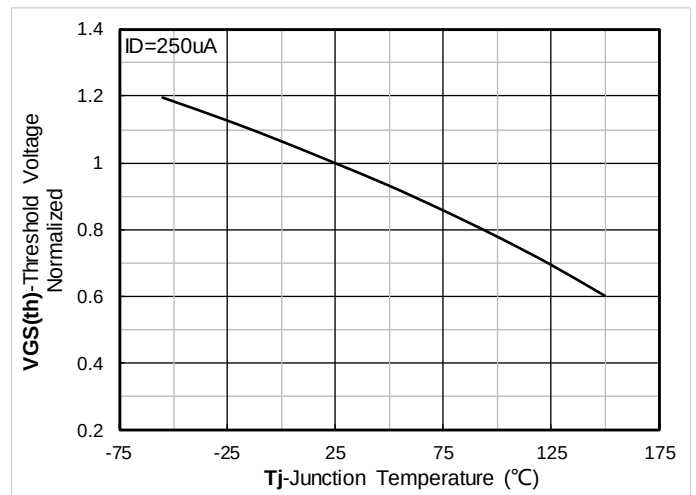


Figure 10. Normalized Threshold voltage

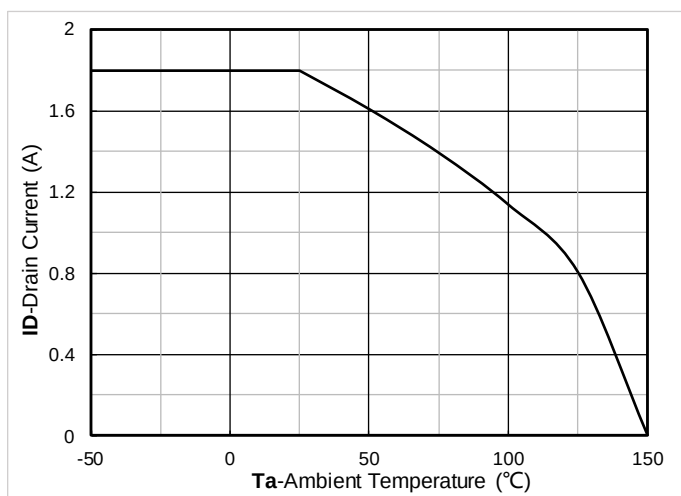


Figure 11. Current dissipation

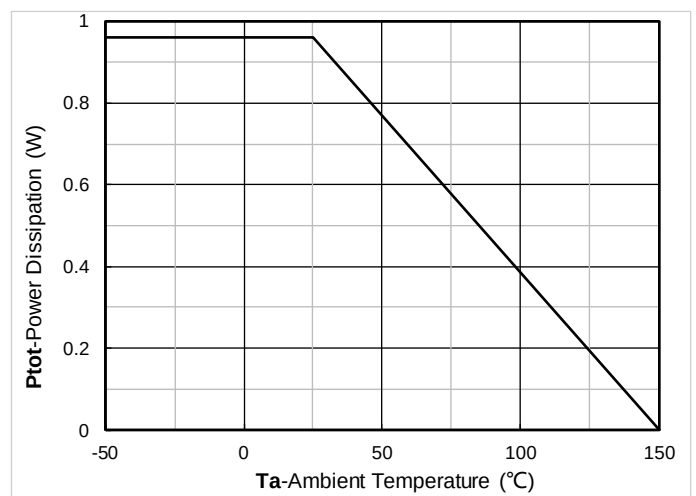


Figure 12. Power dissipation

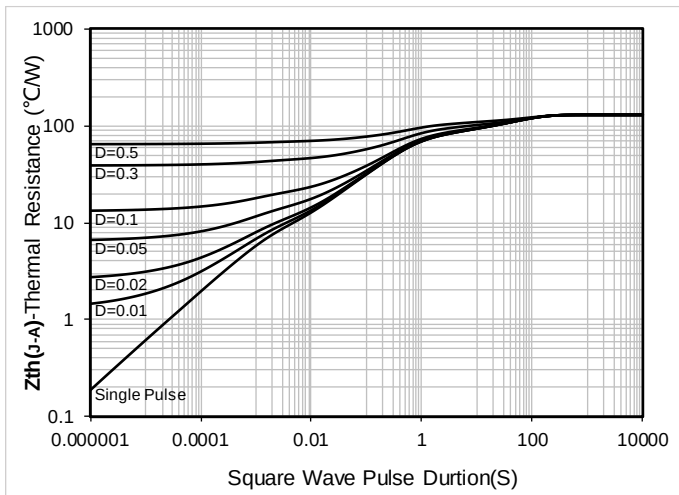


Figure 13. Maximum Transient Thermal Impedance

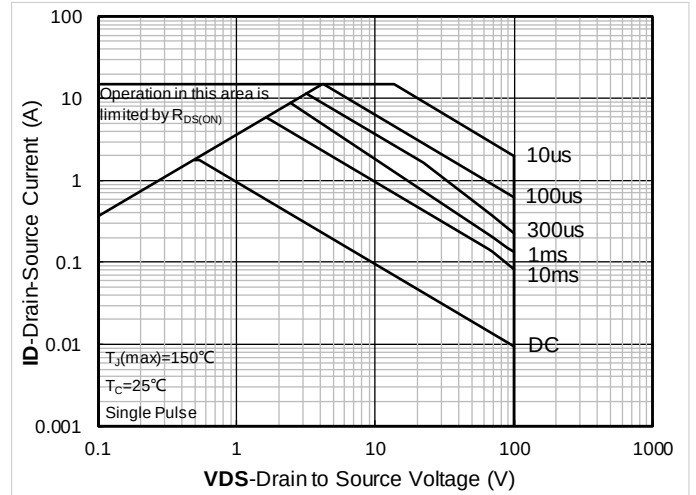


Figure 14. Safe Operation Area

Test Circuits & Waveforms

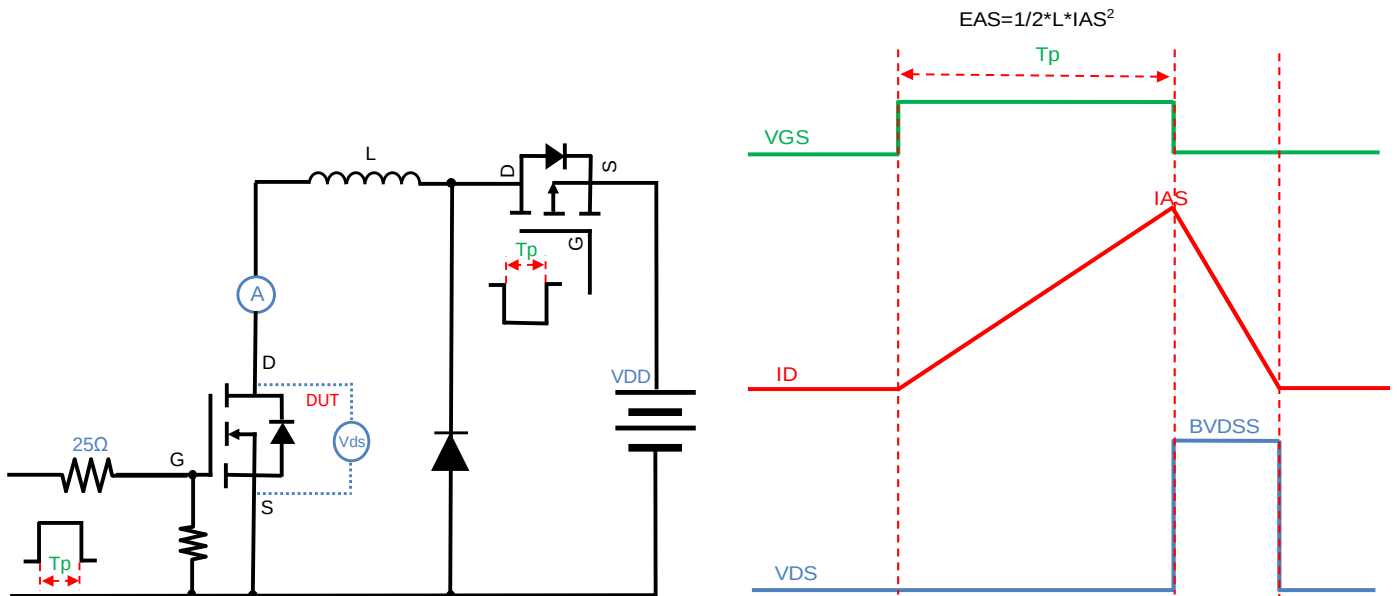


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

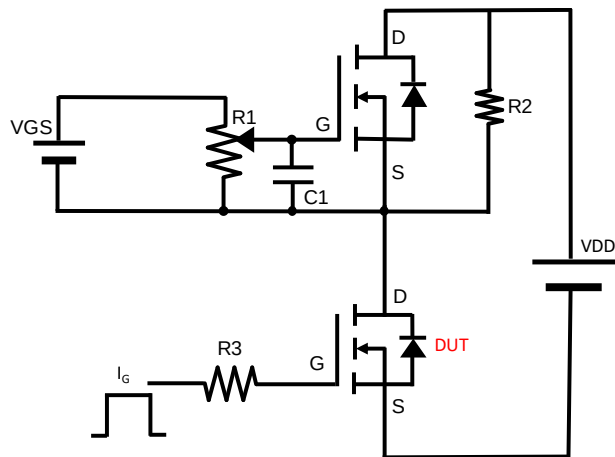


Figure B. Gate Charge Test Circuit & Waveform

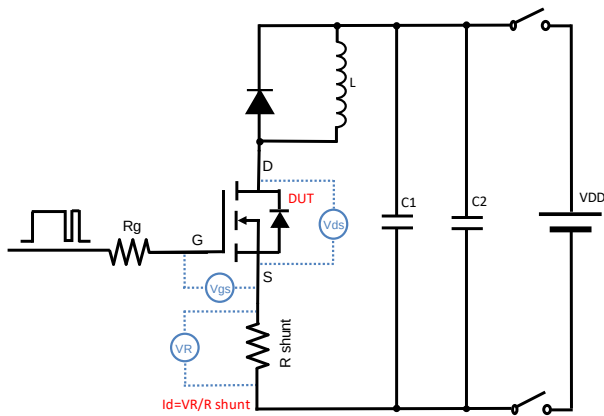


Figure C. Resistive Switching Test Circuit & Waveform

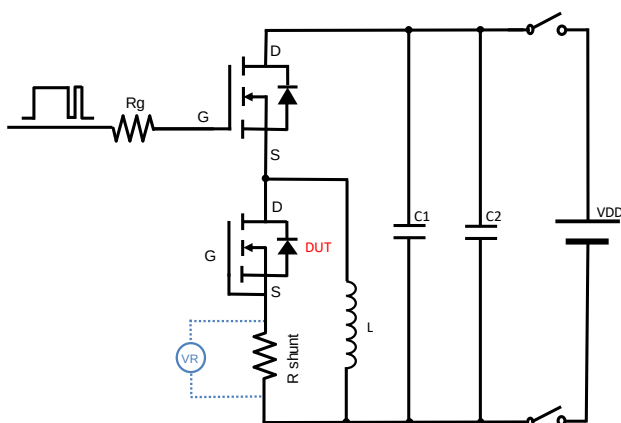
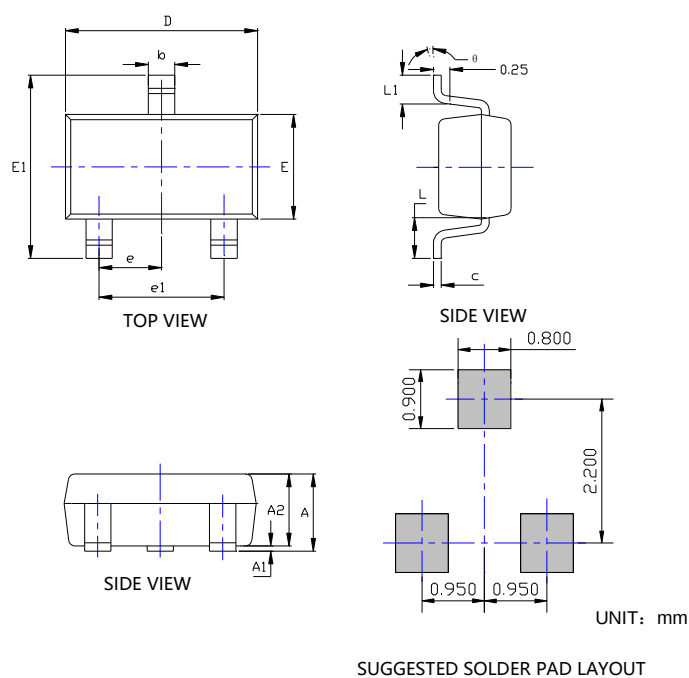


Figure D. Diode Recovery Test Circuit & Waveform

■ SOT-23-3L Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.041	---	0.049	1.050	---	1.250
A1	0.000	---	0.008	0.000	---	0.200
A2	0.041	0.043	0.045	1.050	1.100	1.150
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.111	0.115	0.119	2.820	2.920	3.020
E	0.059	0.063	0.067	1.500	1.600	1.700
E1	0.104	0.110	0.116	2.650	2.800	2.950
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.024REF			0.600REF		
L1	0.012	0.018	0.024	0.300	0.450	0.600
θ	0°	---	8°	0°	---	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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