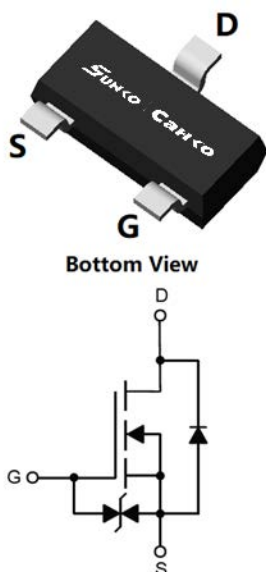
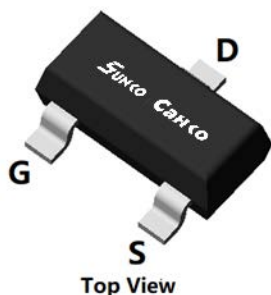


N-Channel Enhancement Mode Field Effect Transistor



SOT-23

Product Summary

- V_{DS} 30V
- I_D 0.4A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.5\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<3\Omega$
- Gate-Source ESD Rating Up to 2KV (HBM)

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	30	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$	I_D	0.4	A
		$T_A=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$		0.25	
Pulsed Drain Current	$T_C=25^{\circ}\text{C}$, $t_p=100\mu\text{s}$		I_{DM}	1.1	A
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$	P_D	0.83	W
		$T_A=100^{\circ}\text{C}$		0.33	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+150	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	125	150	$^\circ\text{C/W}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCL3018KJ	F2	3018KJ.	3000	30000	120000	7" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		V _{DS} =30V, V _{GS} =0V, T _j =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.6	1.1	1.6	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.4A	-	1.6	2.5	Ω
		V _{GS} =4.5V, I _D =0.2A	-	1.95	3	Ω
Diode Forward Voltage	V _{SD}	I _S =0.4A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	390	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	0.4	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	14.6	-	pF
Output Capacitance	C _{oss}		-	3.9	-	
Reverse Transfer Capacitance	C _{rss}		-	2.5	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =0.5A	-	0.85	-	nC
Gate-Source Charge	Q _{gs}		-	0.18	-	
Gate-Drain Charge	Q _{gd}		-	0.38	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.5A, di/dt=100A/us	-	5	-	nC
Reverse Recovery Time	t _{rr}		-	10.6	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =0.5A R _{GEN} =3Ω	-	14.5	-	ns
Turn-on Rise Time	t _r		-	16.9	-	
Turn-off Delay Time	t _{D(off)}		-	14.3	-	
Turn-off fall Time	t _f		-	44.7	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

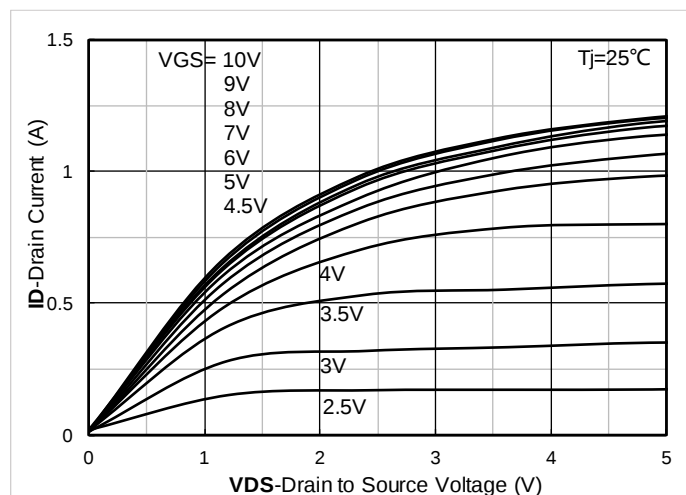


Figure 1. Output Characteristics

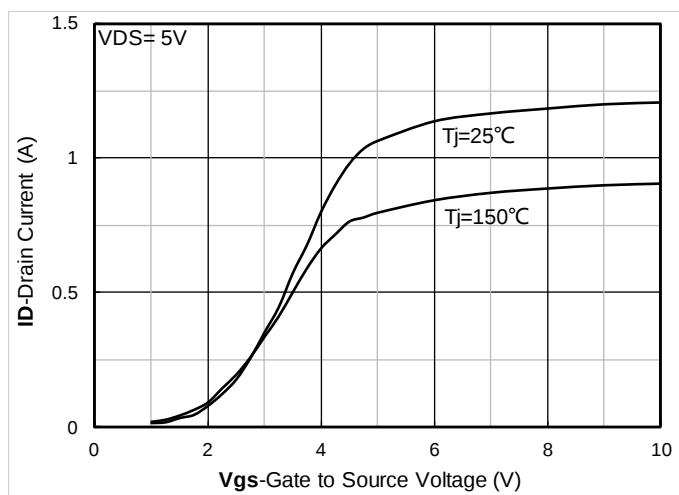


Figure 2. Transfer Characteristics

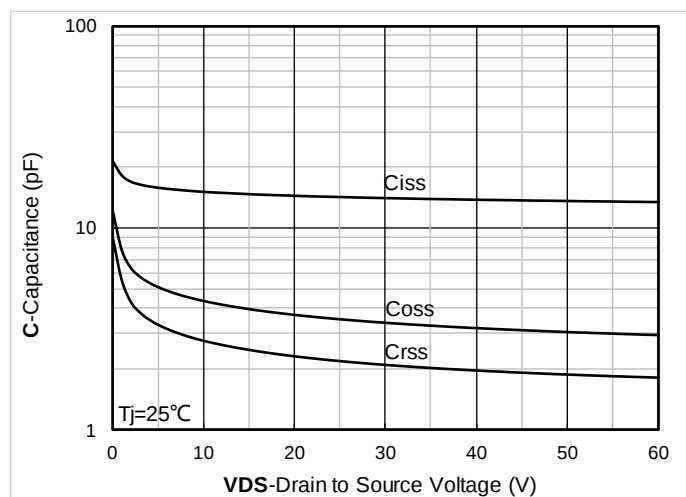


Figure 3. Capacitance Characteristics

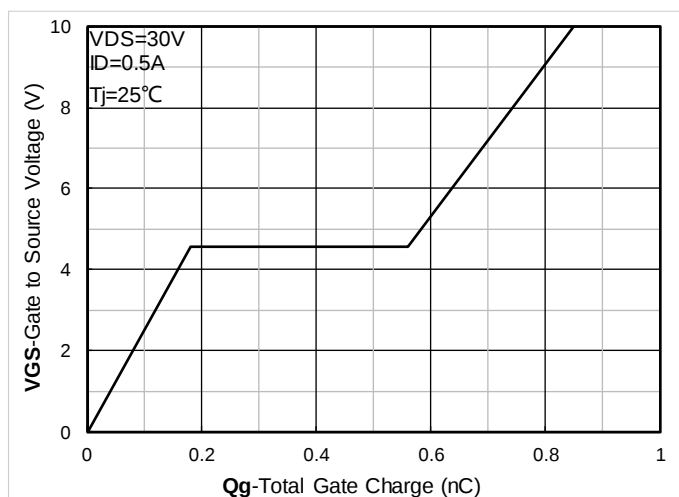


Figure 4. Gate Charge

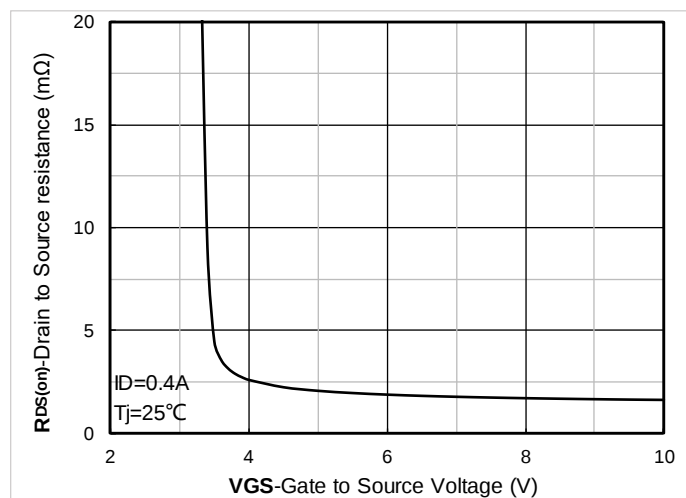


Figure 5. On-Resistance vs Gate to Source Voltage

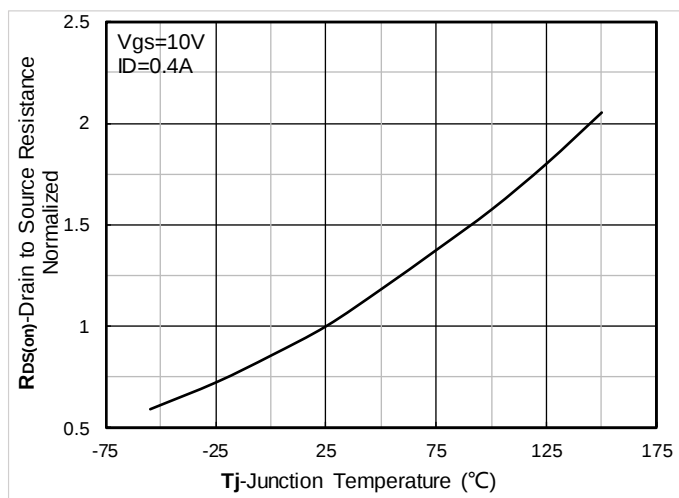


Figure 6. Normalized On-Resistance

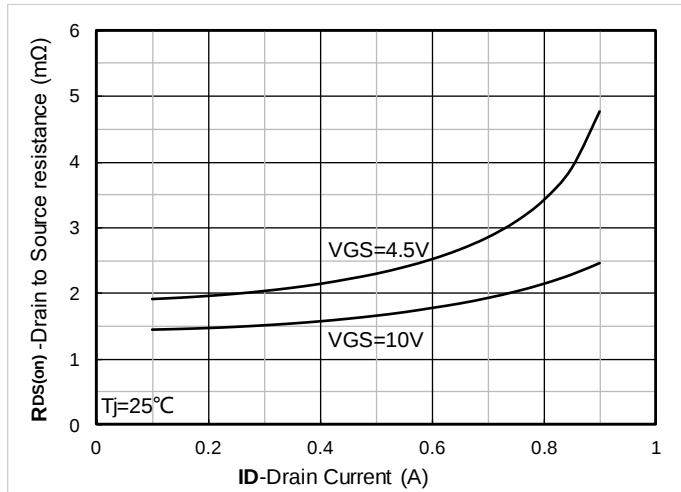


Figure 7. $R_{DS(on)}$ VS Drain Current

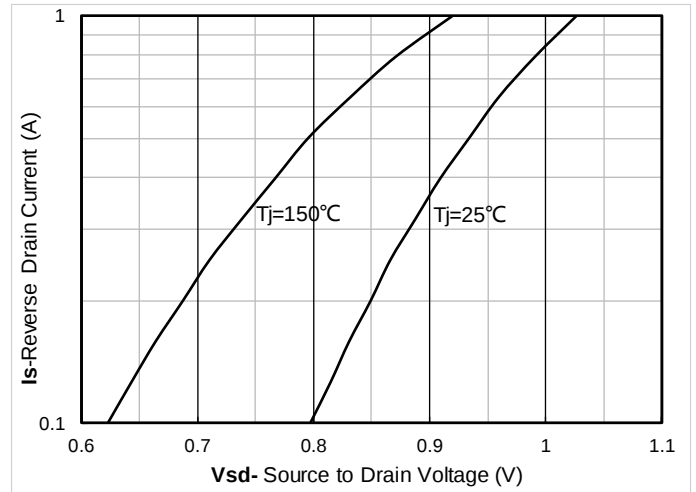


Figure 8. Forward characteristics of reverse diode

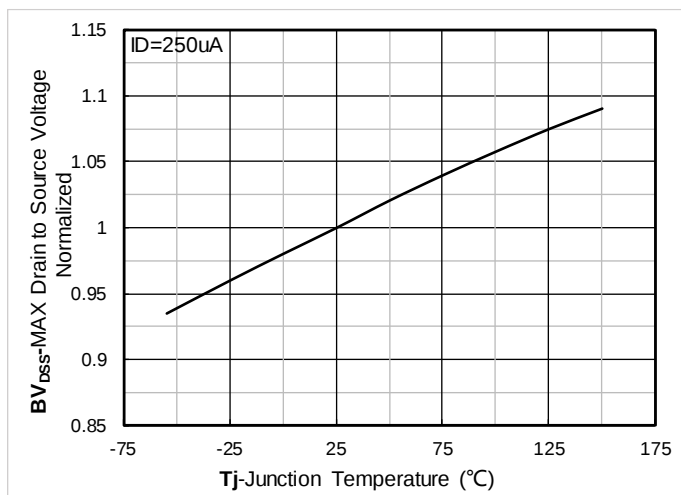


Figure 9. Normalized breakdown voltage

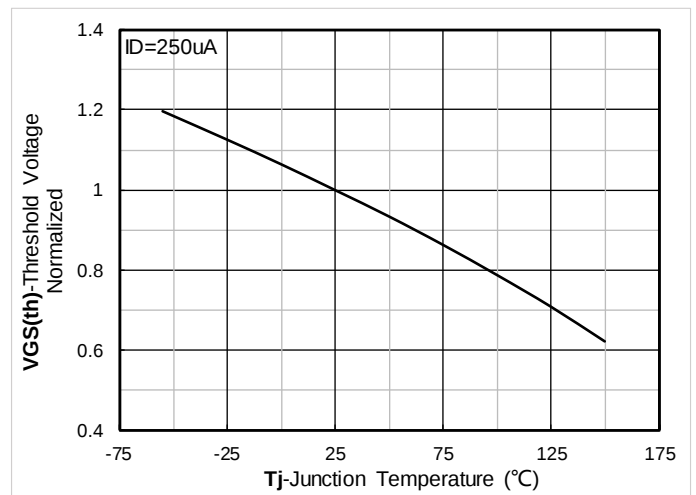


Figure 10. Normalized Threshold voltage

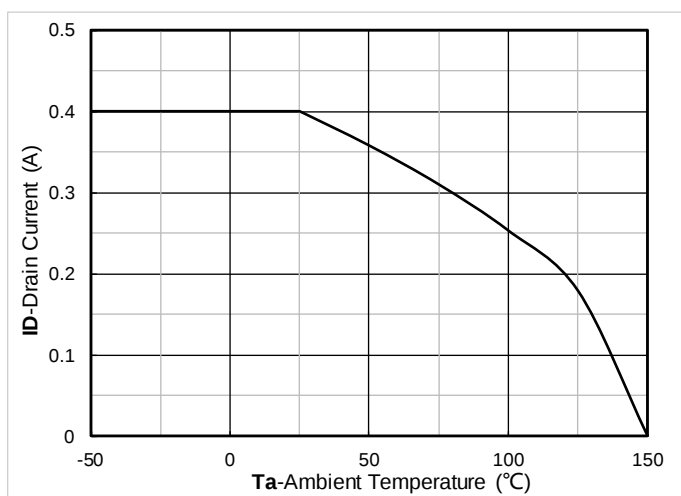


Figure 11. Current dissipation

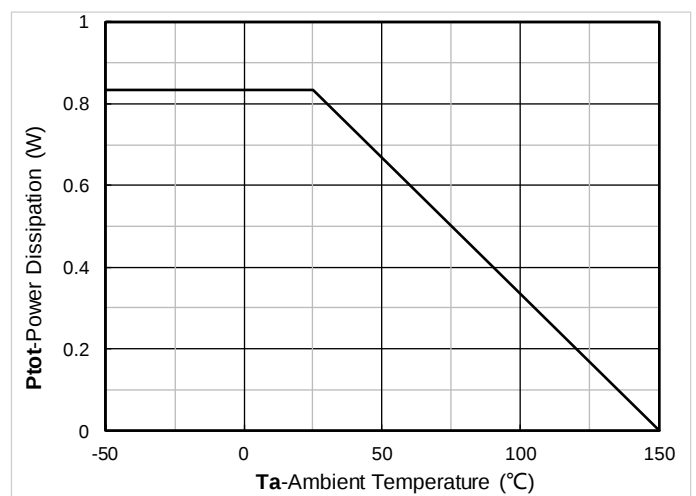


Figure 12. Power dissipation

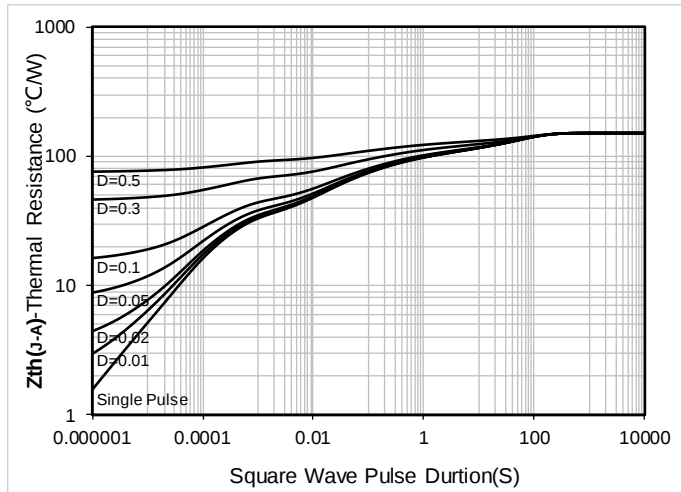


Figure 13. Maximum Transient Thermal Impedance

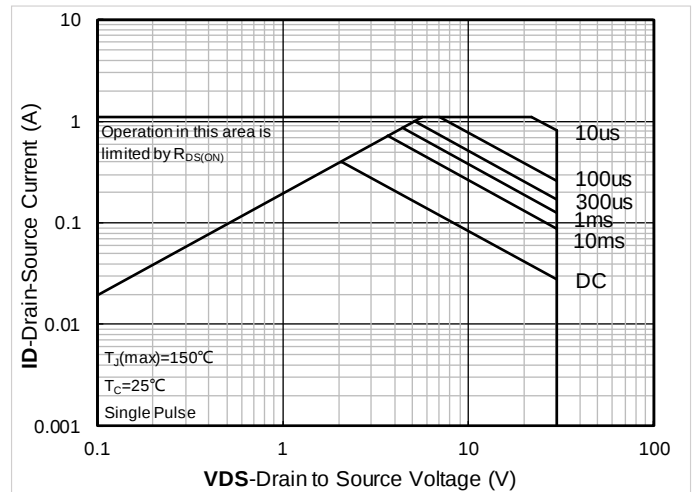


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

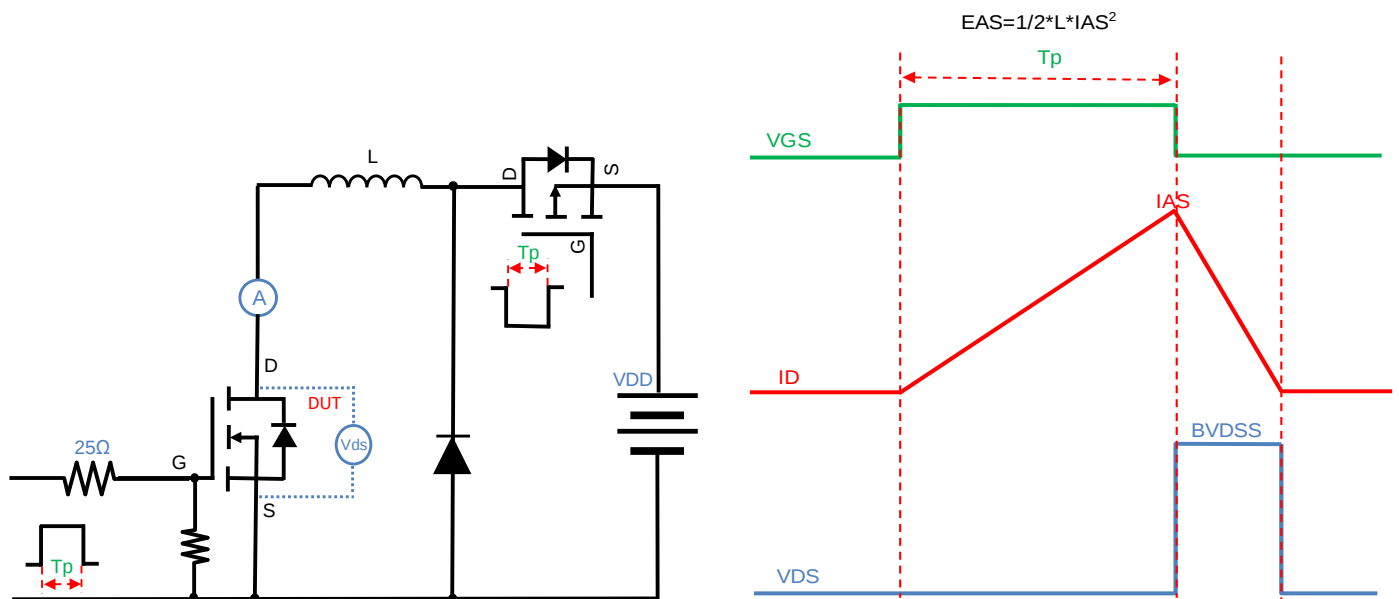


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

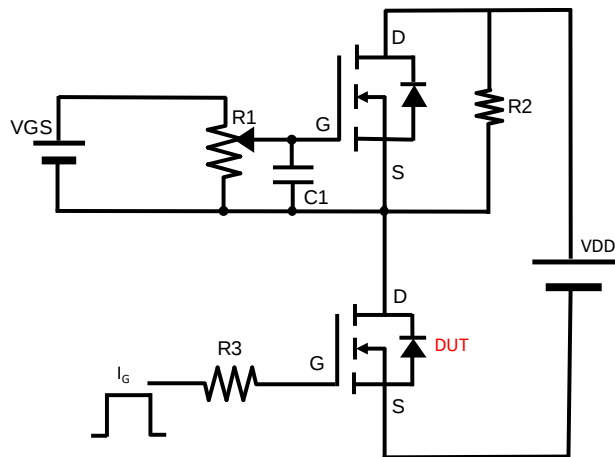


Figure B. Gate Charge Test Circuit & Waveform

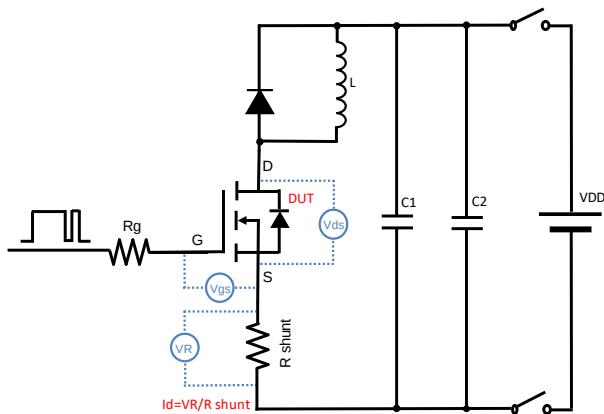


Figure C. Resistive Switching Test Circuit & Waveform

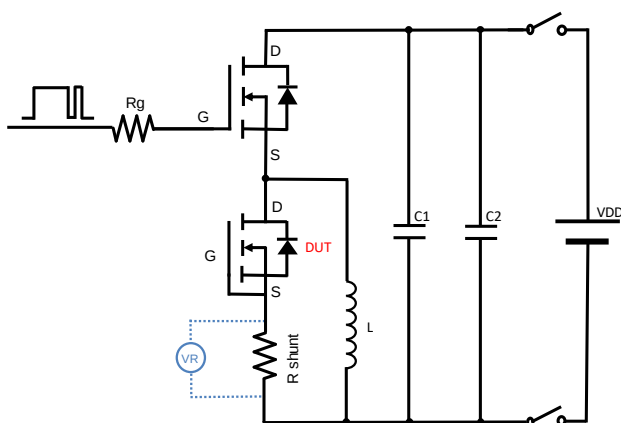
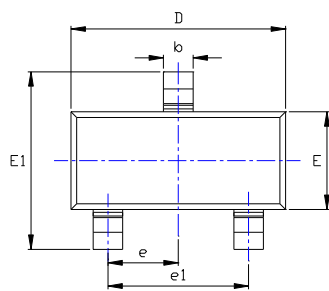
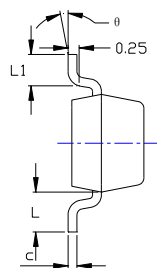


Figure D. Diode Recovery Test Circuit & Waveform

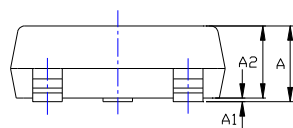
■ SOT-23 Package information



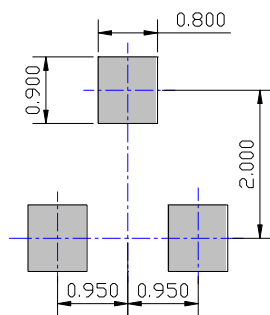
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037 TYP		0.950 TYP	
e1	0.071	0.079	1.800	2.000
L	0.022 REF		0.550 REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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