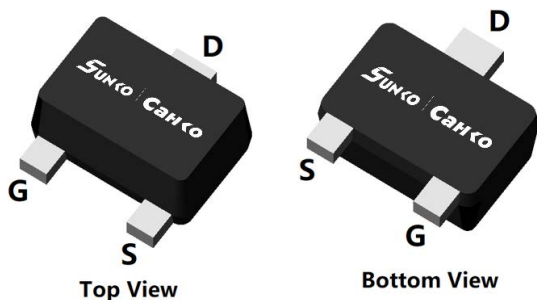
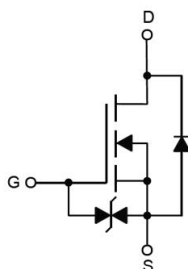


N-Channel Enhancement Mode Field Effect Transistor



SOT-723



Product Summary

- V_{DS} 30 V
- I_D 300mA
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $< 2.5\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $< 3\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) $< 8\Omega$

General Description

- Trench Power LV MOSFET technology
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Portable equipment

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	300	mA
	$T_A=100^\circ\text{C}$		190	
Pulsed Drain Current ^A		I_{DM}	800	mA
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$	P_D	270	mW
	$T_A=100^\circ\text{C}$		105	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^C	Steady-State	$R_{\theta JA}$	370	460	$^\circ\text{C/W}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCL3541KTJ	F2	KNA	8000	80000	320000	7" reel

SCL3541KTJ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		V _{DS} =30V, V _{GS} =0V, T _j =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±10	uA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.6	1.0	1.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =300mA	-	1.6	2.5	Ω
		V _{GS} =4.5V, I _D =200mA	-	1.8	3	
		V _{GS} =2.5V, I _D =100mA	-	4.5	8	
Diode Forward Voltage	V _{SD}	I _S =300mA, V _{GS} =0V	-	0.9	1.3	V
Gate resistance	R _G	f=1MHz	-	150	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	300	mA
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz	-	28	-	pF
Output Capacitance	C _{oss}		-	7.8	-	
Reverse Transfer Capacitance	C _{rss}		-	6.5	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =0.3A	-	1.2	-	nC
Gate-Source Charge	Q _{gs}		-	0.2	-	
Gate-Drain Charge	Q _{gd}		-	0.1	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.3A, di/dt=100A/us	-	3	-	nC
Reverse Recovery Time	t _{rr}		-	9	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =10V, I _D =0.3A R _{GEN} =3.9Ω	-	2.8	-	ns
Turn-on Rise Time	t _r		-	7.9	-	
Turn-off Delay Time	t _{D(off)}		-	2.6	-	
Turn-off fall Time	t _f		-	9.9	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

C. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

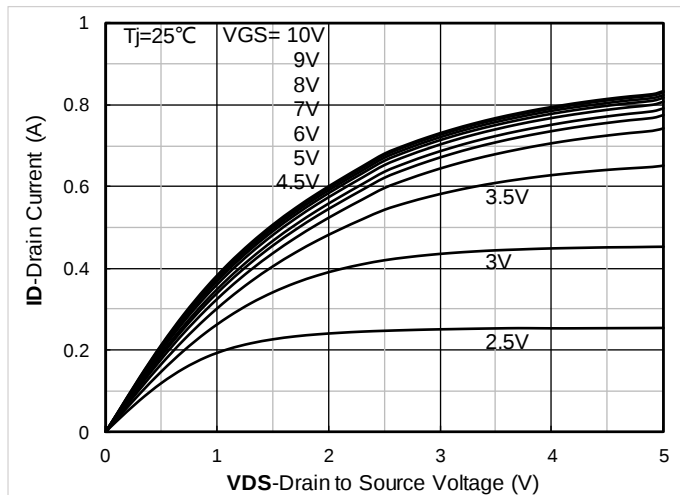


Figure 1. Output Characteristics

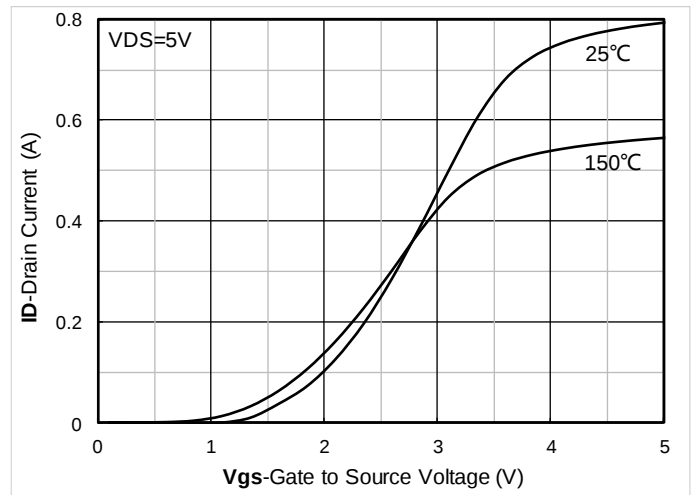


Figure 2. Transfer Characteristics

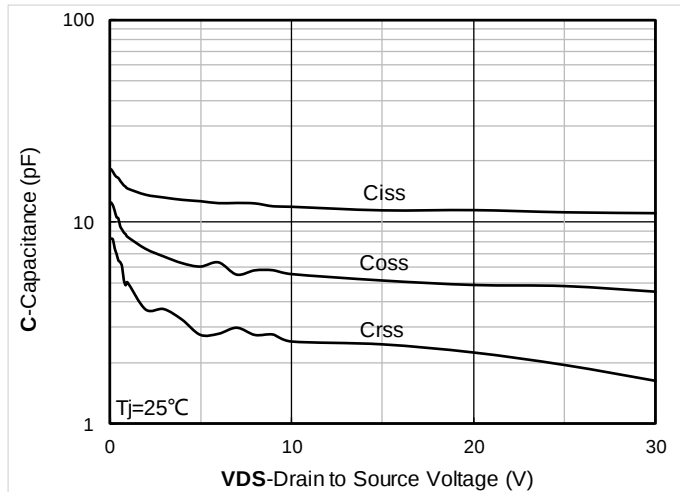


Figure 3. Capacitance Characteristics

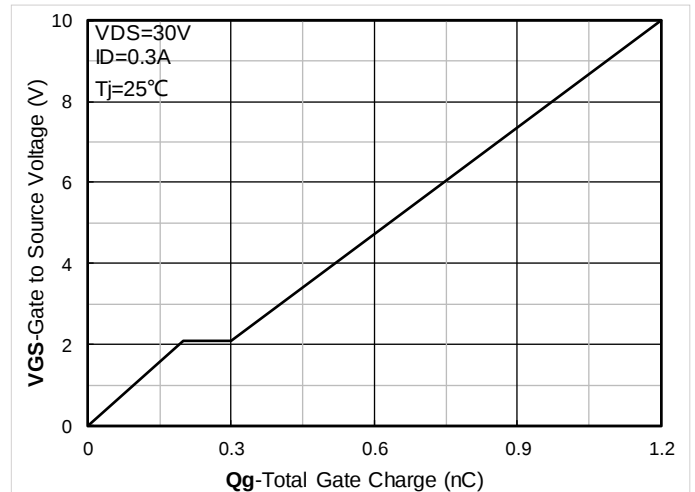


Figure 4. Gate Charge

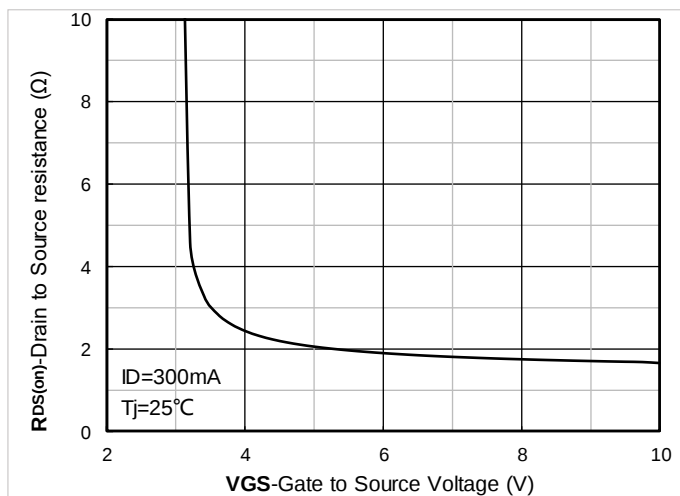


Figure 5. On-Resistance vs Gate to Source Voltage

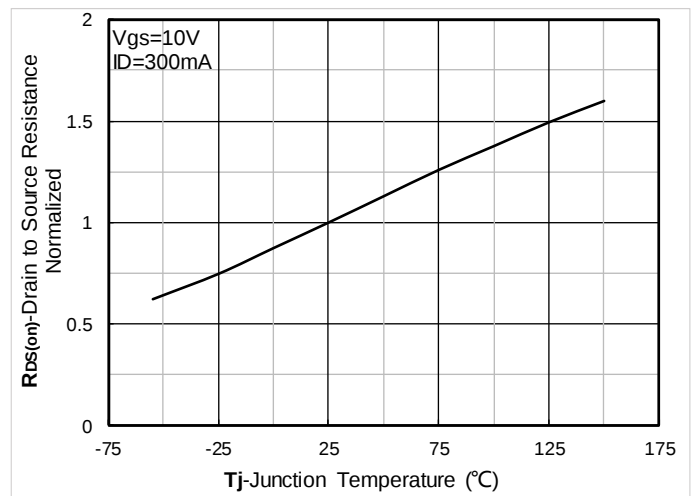


Figure 6. Normalized On-Resistance

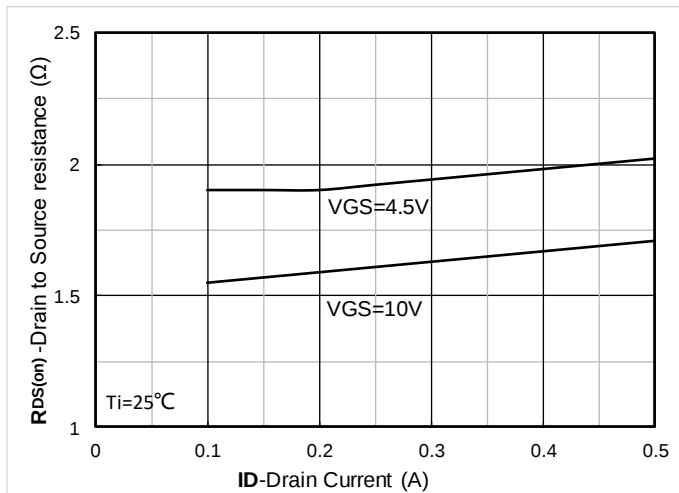


Figure 7. $R_{DS(on)}$ VS Drain Current

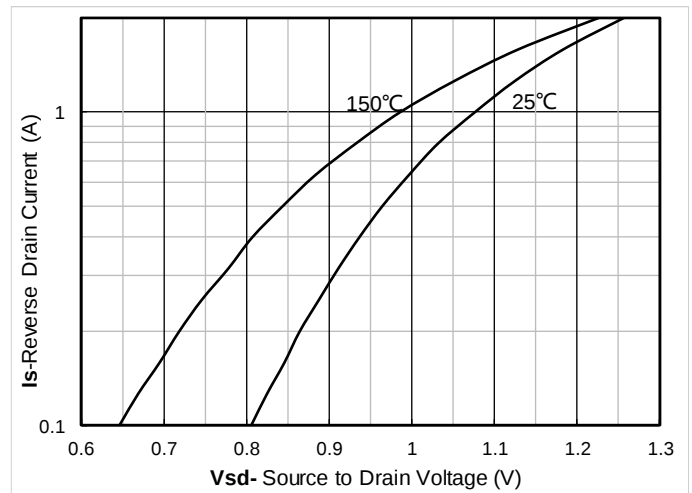


Figure 8. Forward characteristics of reverse diode

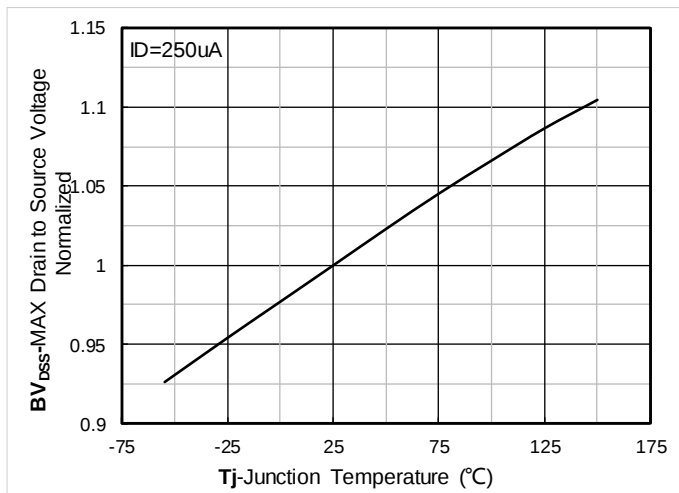


Figure 9. Normalized breakdown voltage

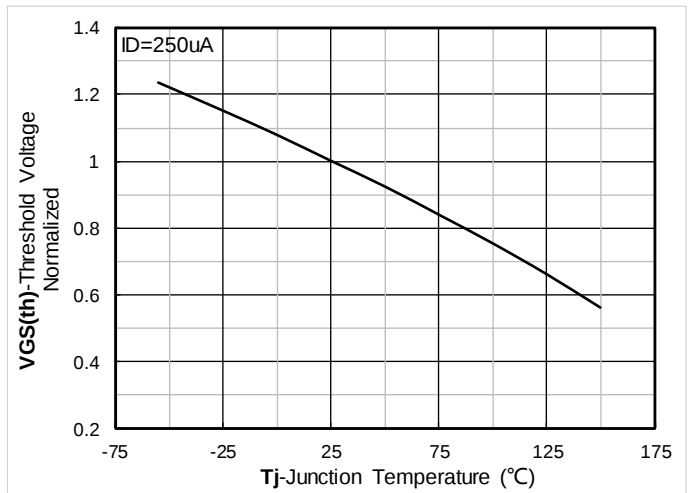


Figure 10. Normalized Threshold voltage

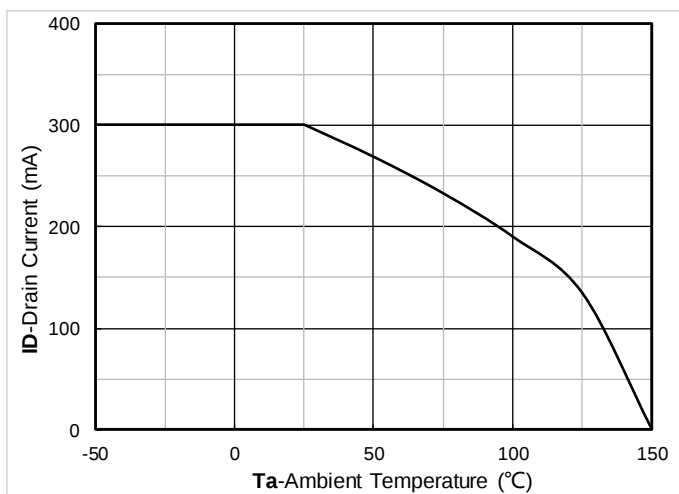


Figure 11. Current dissipation

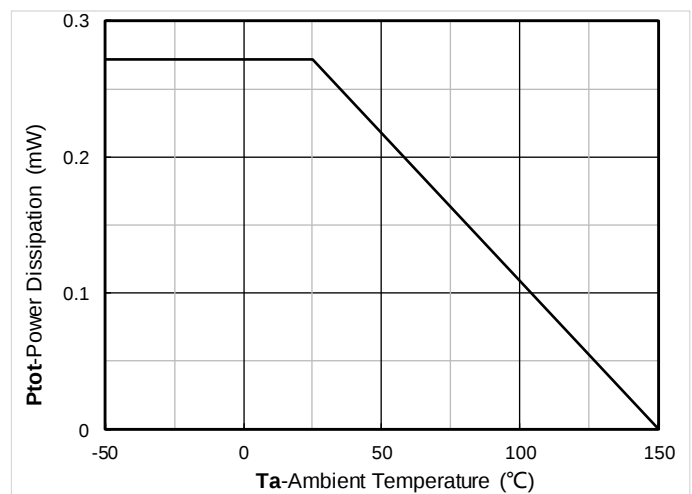


Figure 12. Power dissipation

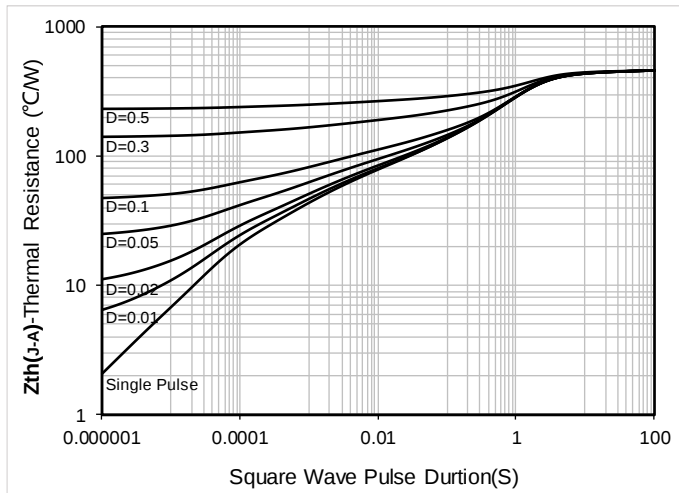


Figure 13. Maximum Transient Thermal Impedance

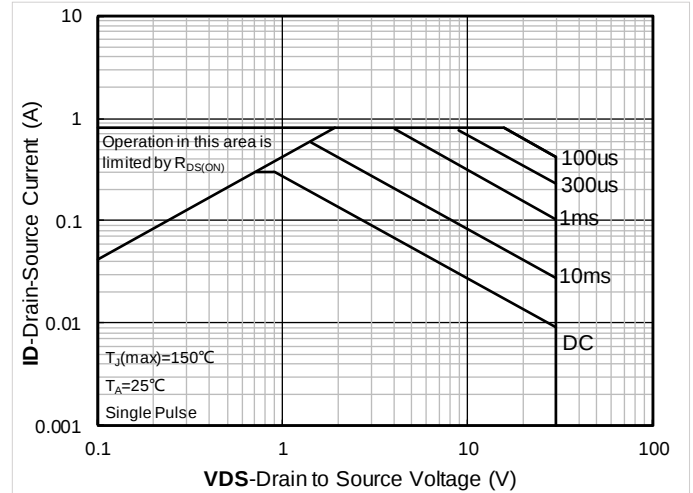


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

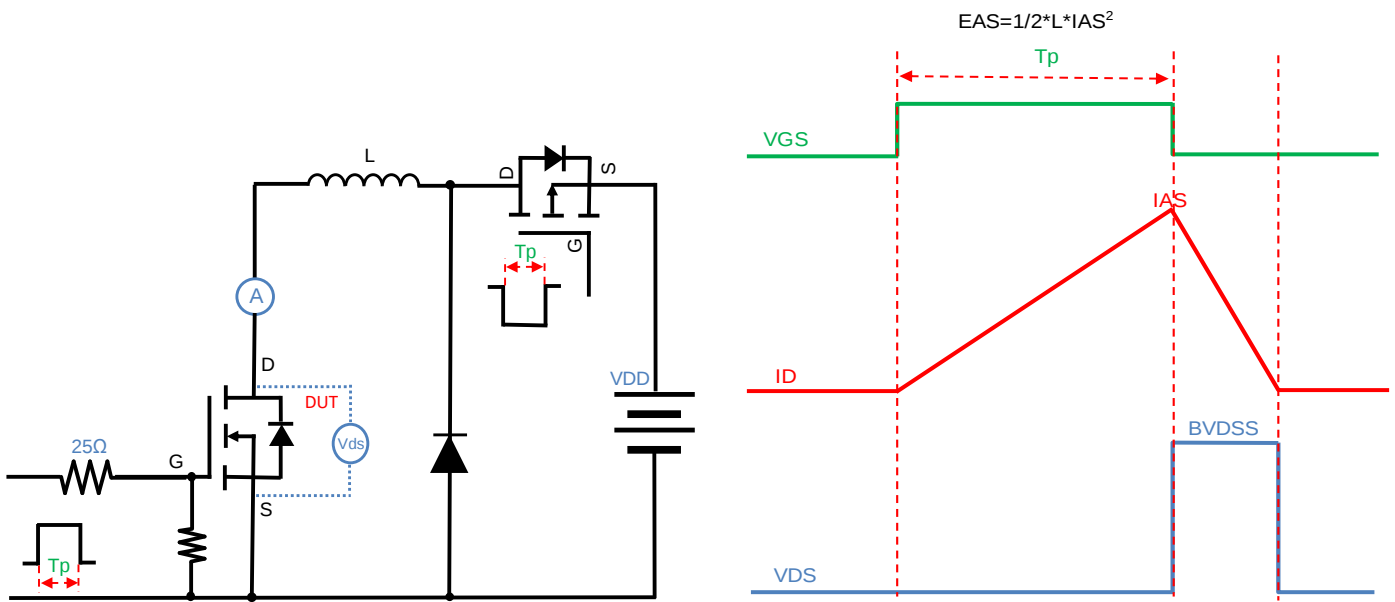


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform

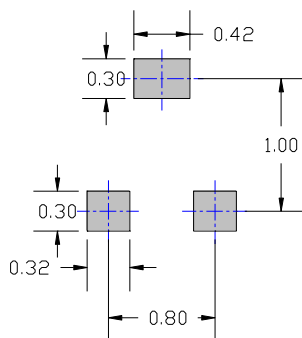
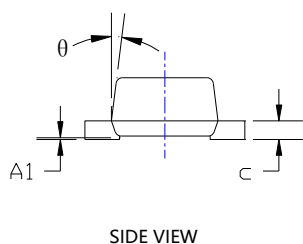
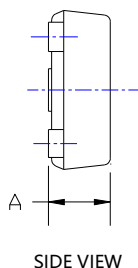
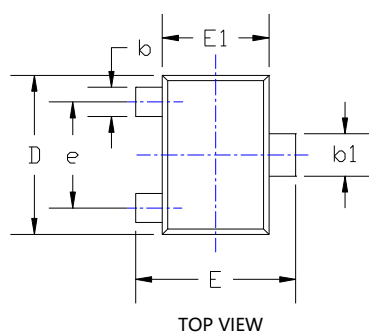


Figure C. Resistive Switching Test Circuit & Waveform



Figure D. Diode Recovery Test Circuit & Waveform

■ SOT-723 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031 TYP.		0.800 TYP.	
θ	7° REF.		7° REF.	

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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