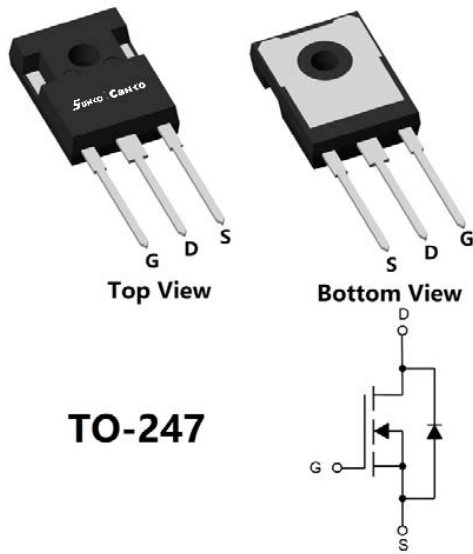


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 600V
- I_D 33A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<72m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- EV Charger
- AC-DC Power Management
- Sever/Telecom/PC Power

■ Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V _{DS}	600	V
Gate-source Voltage			V _{GS}	±30	V
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25℃	I _D	3.9	A
		T _A =100℃		2.4	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25℃		33	
		T _C =100℃		20	
Pulsed Drain Current	T _C =25℃, t _p =100μs		I _{DM}	110	A
Avalanche energy	V _G =10V, R _G =25Ω, L=30mH, I _{AS} =7.7A		EAS	889.35	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25℃	P _D	3.1	W
		T _A =100℃		1.2	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25℃		227	
		T _C =100℃		90	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55~+150	℃

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	35	40	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.45	0.55	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCN48C60HJ	B1	SCN48C60HJ	30	360	1800	Tube

SCN48C60HJ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	600	-	-	V
		V _{GS} = 0V, I _D =10mA	600	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	-	-	10	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±30V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	3	4	5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =24A	-	60	72	mΩ
Diode Forward Voltage	V _{SD}	I _S =24A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	2.2	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	33	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =300V, V _{GS} =0V, f=1MHz	-	3480	-	pF
Output Capacitance	C _{oss}		-	108	-	
Reverse Transfer Capacitance	C _{rss}		-	22.4	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =300V, I _D =24A	-	70	-	nC
Gate-Source Charge	Q _{gs}		-	21.8	-	
Gate-Drain Charge	Q _{gd}		-	29.6	-	
Reverse Recovery Charge	Q _{rr}	I _F =24A, di/dt=100A/us	-	1430	-	nC
Reverse Recovery Time	t _{rr}		-	157	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =300V, I _D =24A R _{GEN} =3Ω	-	64	-	ns
Turn-on Rise Time	t _r		-	18.5	-	
Turn-off Delay Time	t _{D(off)}		-	41.5	-	
Turn-off fall Time	t _f		-	6	-	

- Note:
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
 2. The value of R_{θJA} is measured in the still air environment with TA =25°C.The maximum allowed junction temperature of 150°C.
 3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

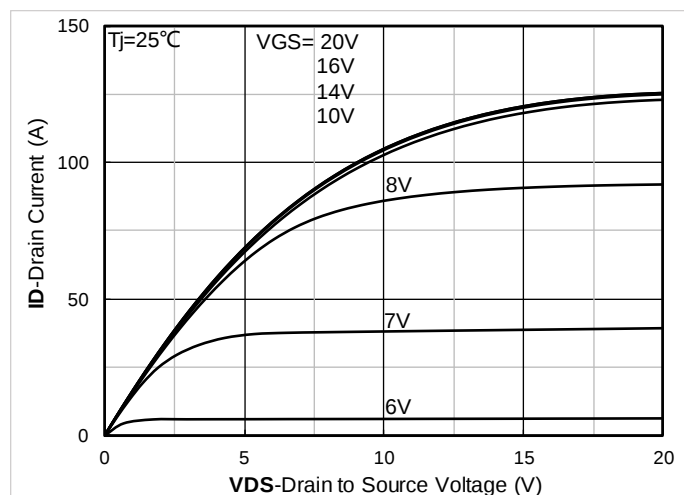


Figure 1. Output Characteristics

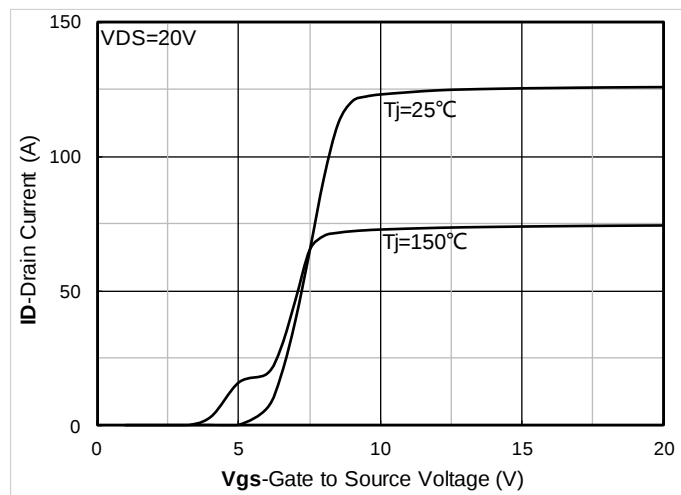


Figure 2. Transfer Characteristics

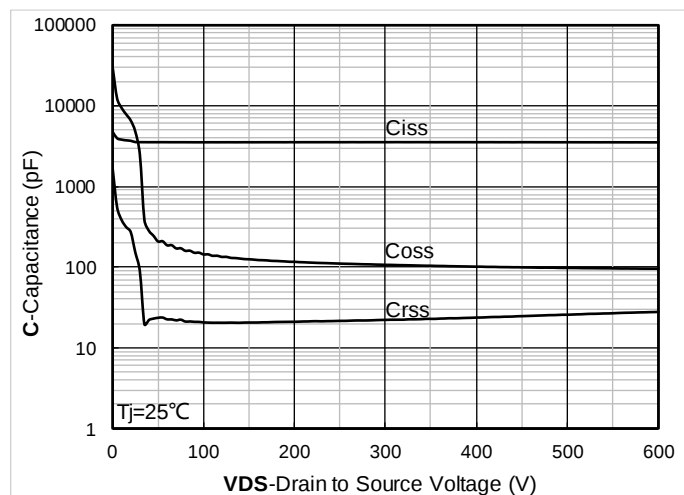


Figure 3. Capacitance Characteristics

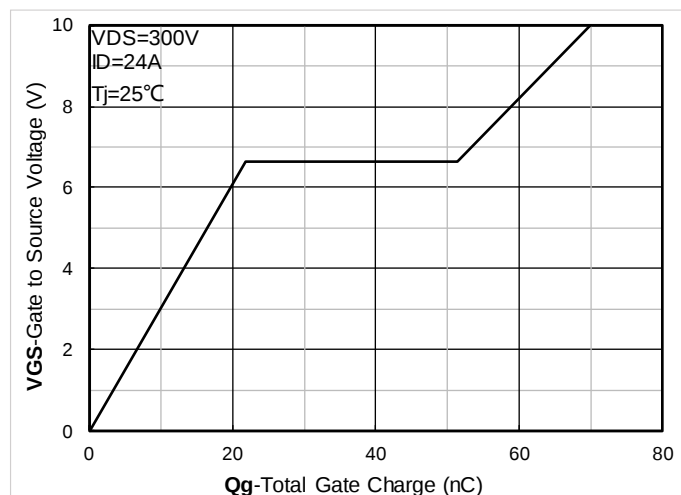


Figure 4. Gate Charge

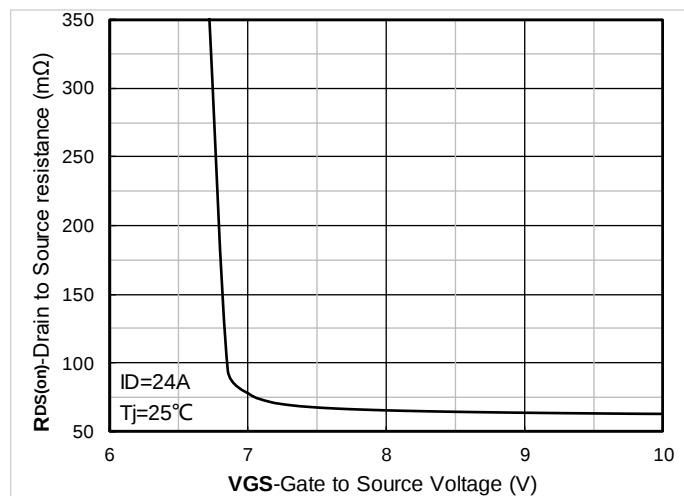


Figure 5. On-Resistance vs Gate to Source Voltage

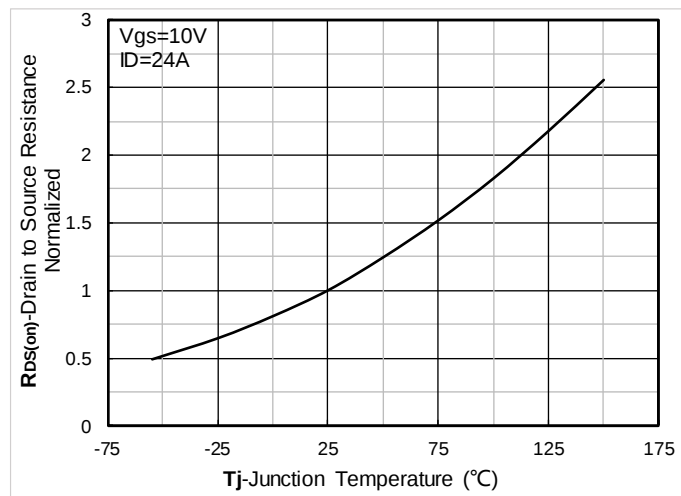


Figure 6. Normalized On-Resistance

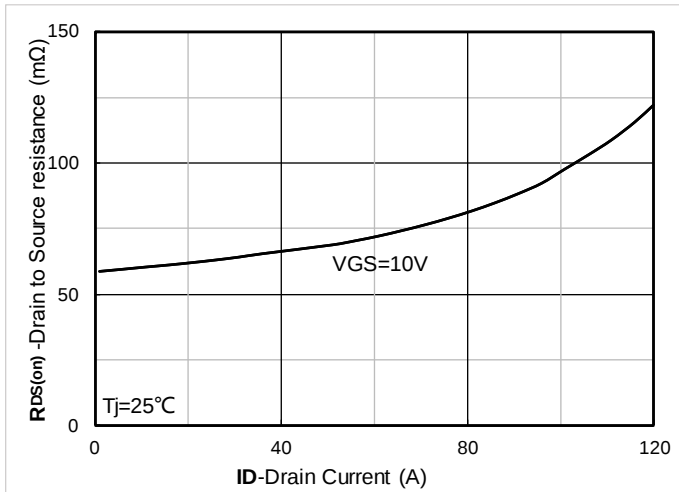


Figure 7. $R_{DS(on)}$ VS Drain Current

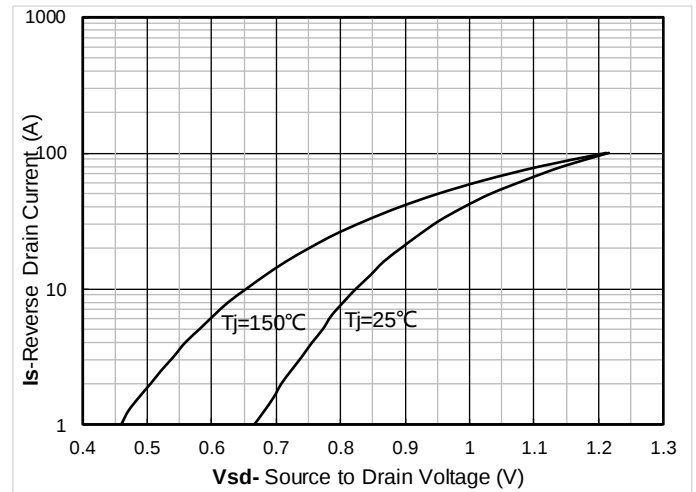


Figure 8. Forward characteristics of reverse diode

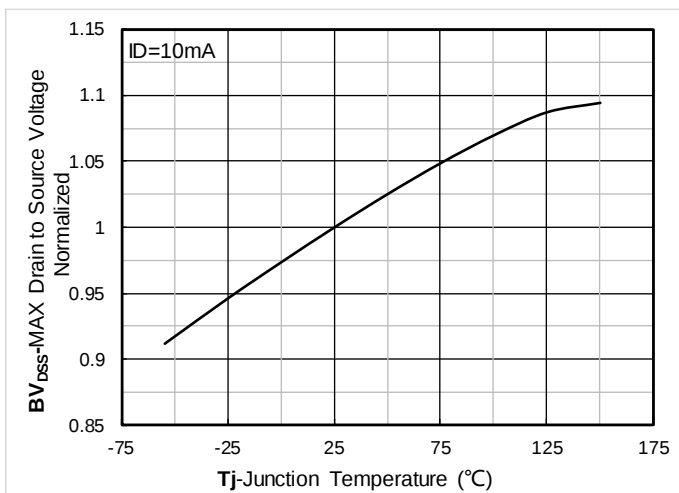


Figure 9. Normalized breakdown voltage

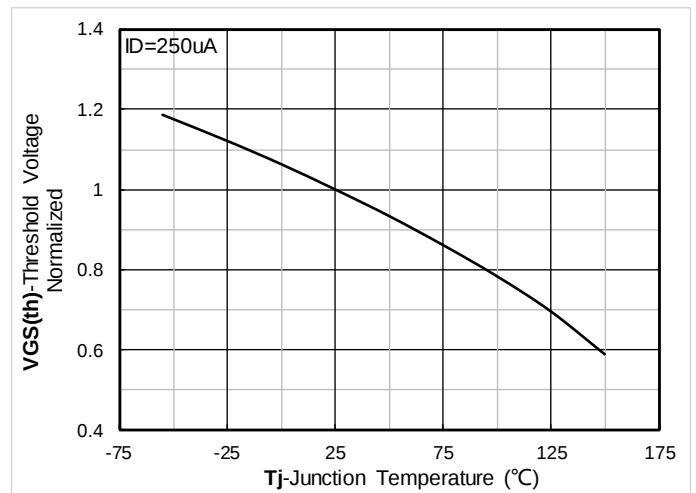


Figure 10. Normalized Threshold voltage

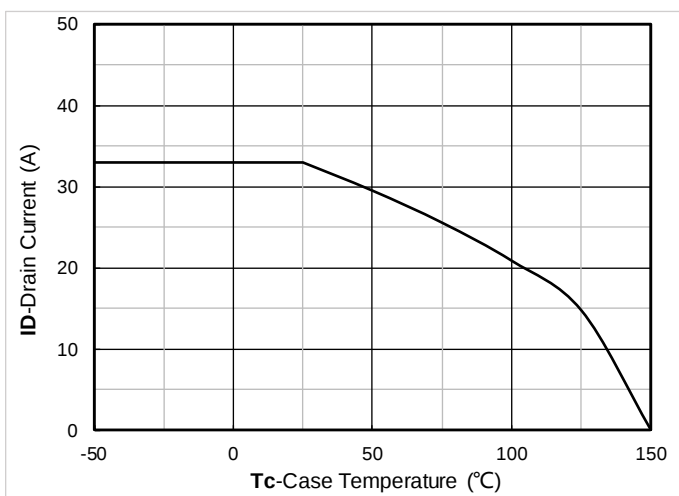


Figure 11. Current dissipation

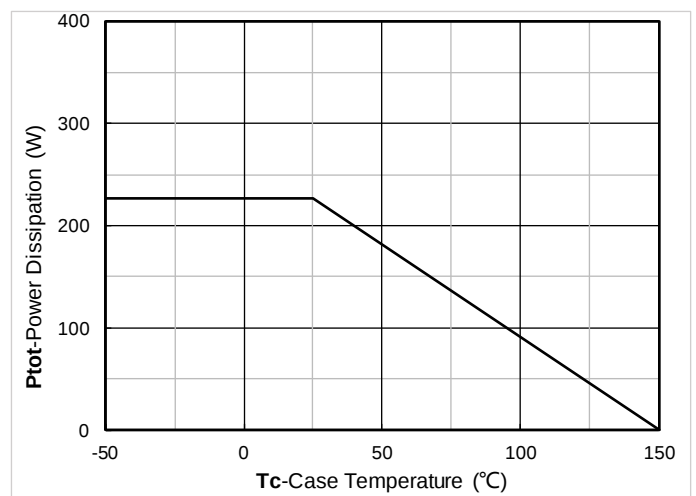


Figure 12. Power dissipation

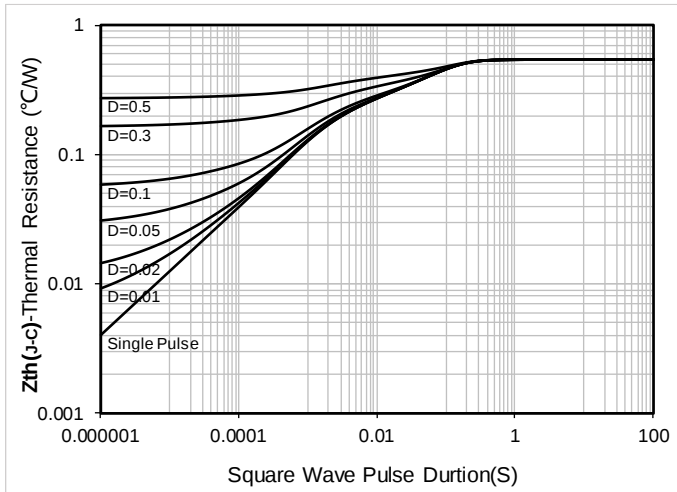


Figure 13. Maximum Transient Thermal Impedance

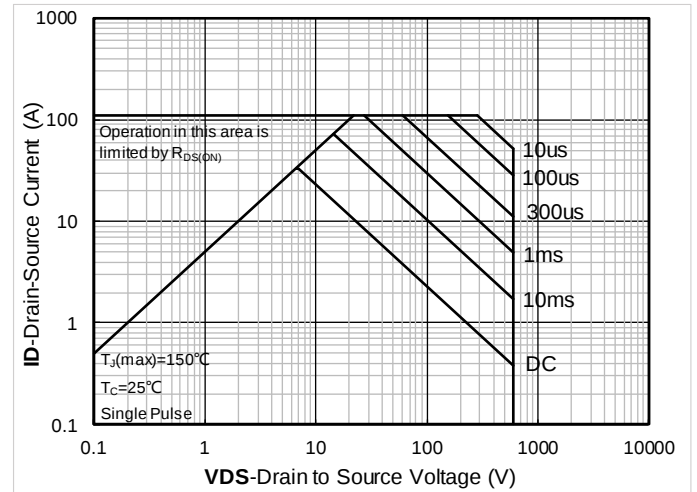


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

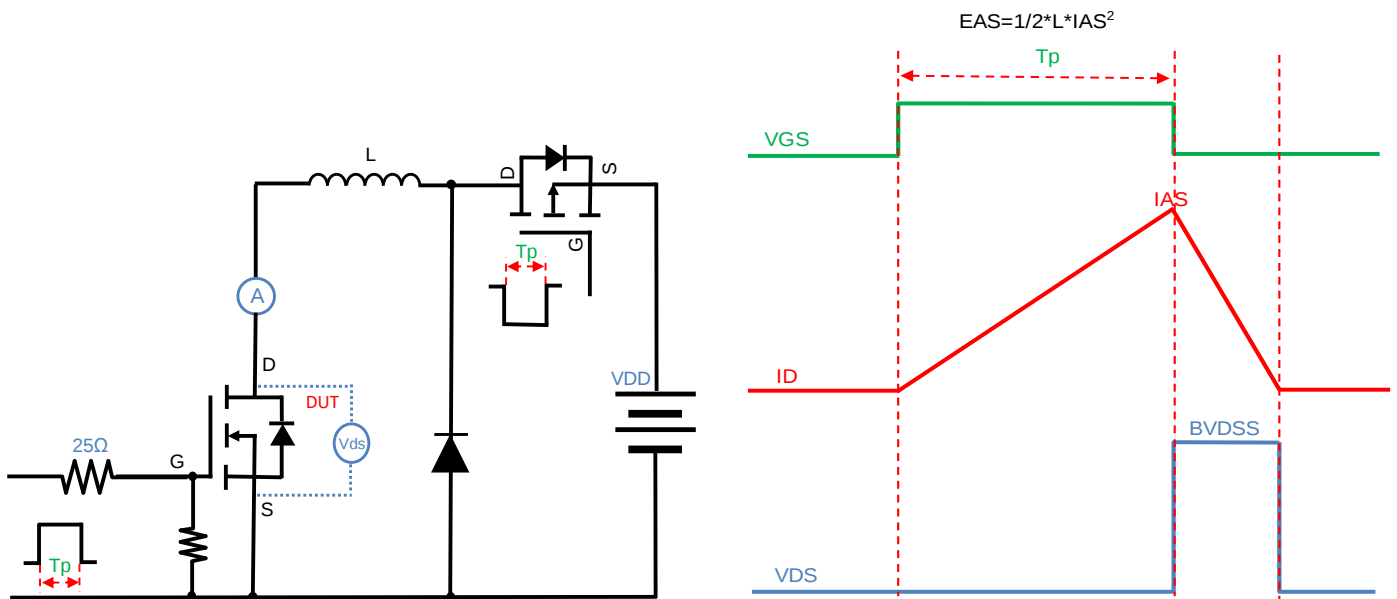


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform



Figure C. Resistive Switching Test Circuit & Waveform

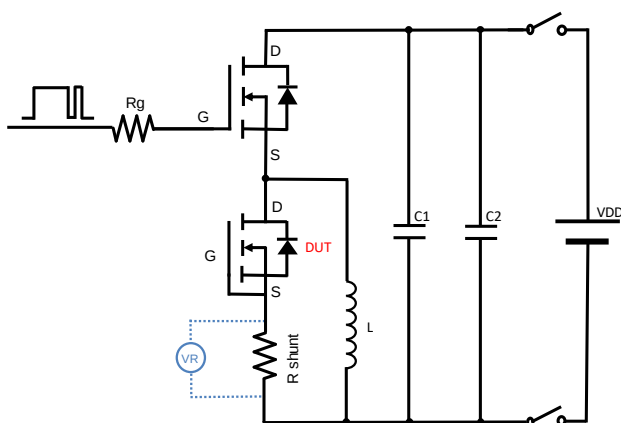
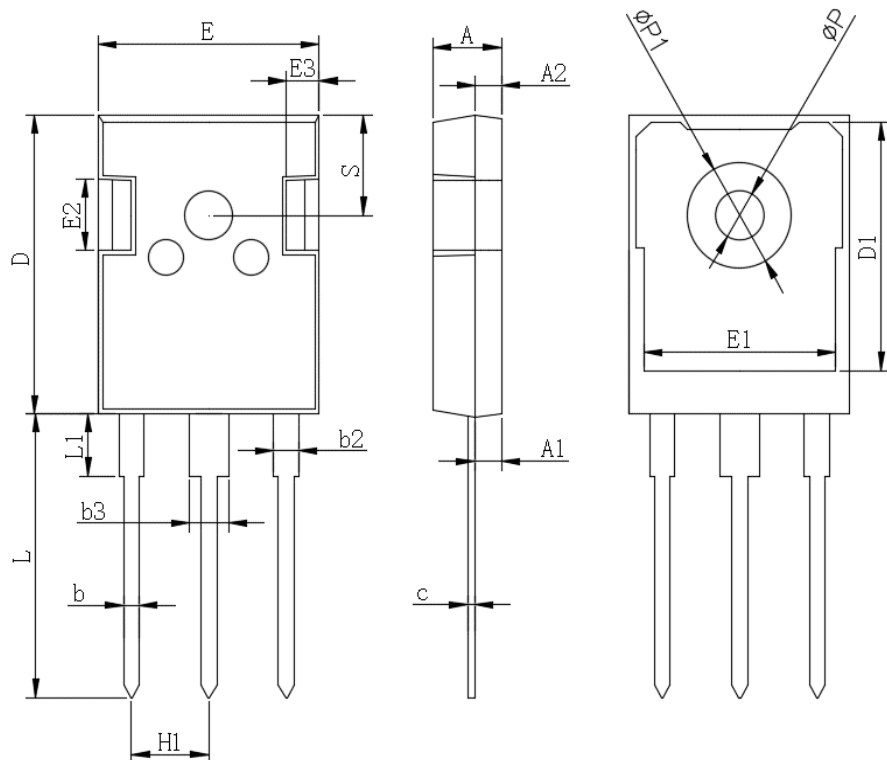


Figure D. Diode Recovery Test Circuit & Waveform

■ TO-247AB Package information

TO-247AB



TO-247AB		
Dim	Min	Max
A	4.80	5.20
A1	2.21	2.61
A2	1.85	2.15
b	1.0	1.4
b2	1.91	2.21
c	0.5	0.7
D	20.70	21.30
D1	16.25	16.85
E	15.50	16.10
E1	13.0	13.6
E2	4.80	5.20
E3	2.30	2.70
L	19.62	20.22
L1	-	4.30
ØP	3.40	3.80
ØP1	-	7.30
S	6.15TYP	
H1	5.44TYP	
b3	2.80	3.20

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