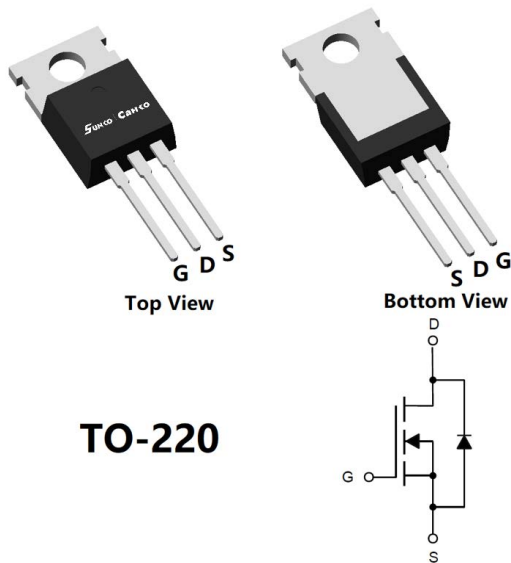


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 190A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<3.1m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switch
- Battery management
- Solar

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	100	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} = 10V	I _D	-	24.1	A
		T _A =100°C,V _{GS} = 10V		-	17	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} = 10V,Chip limitation		-	190	
		T _C =100°C,V _{GS} = 10V		-	134	
Pulsed Drain Current	T _C =25 °C ,t _p ≤10μs		I _{DM}	-	760	
Maximum Body-Diode Continuous Current	T _C =25 °C		I _S		175	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =50.3A		EAS	-	632.52	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	3.75	W
		T _A =100°C		-	1.87	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	230	
		T _C =100°C		-	115	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	40	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.65	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCP3D1G10H	B1	SCP3D1G10H	50	/	5000	Tube

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _j =25℃	100	-	-	V
		V _{GS} =0V, I _D =1mA, T _j =25℃	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _j =25℃	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =125℃	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25℃	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _j =25℃	2.1	2.9	3.7	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A, T _j =25℃	-	2.5	3.1	mΩ
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V, T _j =25℃	-	0.84	1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25℃	-	2.3	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=0.5MHz, T _j =25℃	-	7076	-	pF
Output Capacitance	C _{oss}		-	2348	-	
Reverse Transfer Capacitance	C _{rss}		-	42	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A, T _j =25℃	-	94	-	nC
Gate-Source Charge	Q _{gs}		-	30.5	-	
Gate-Drain Charge	Q _{gd}		-	15	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/μs, V _{GS} =0V, V _R =50V, T _j =25℃	-	50	-	nC
Reverse Recovery Time	t _{rr}		-	48	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =50V, I _D =50A, R _L =1Ω, R _{GEN} =3Ω, T _j =25℃	-	29	-	ns
Turn-on Rise Time	t _r		-	54	-	
Turn-off Delay Time	t _{D(off)}		-	67	-	
Turn-off Fall Time	t _f		-	42	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $175^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

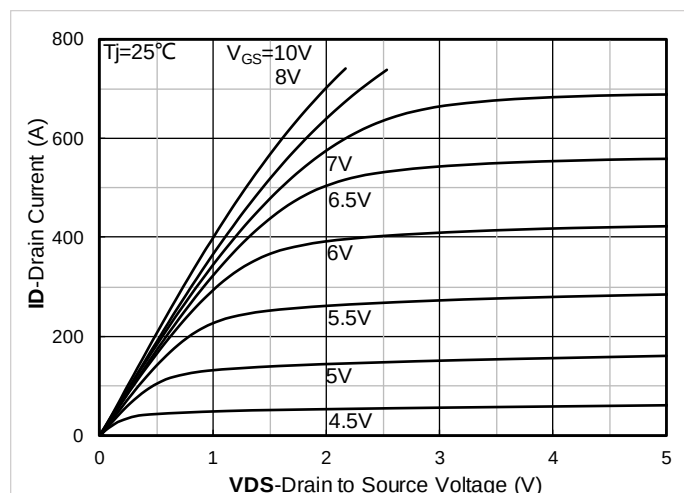


Figure 1. Output Characteristics; typical values

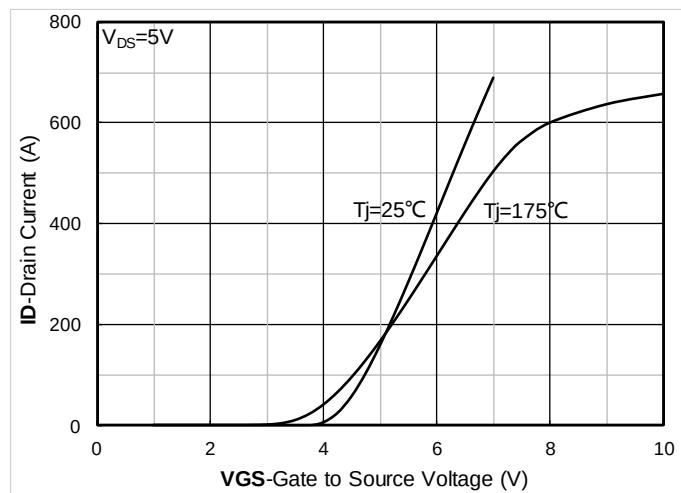


Figure 2. Transfer Characteristics; typical values

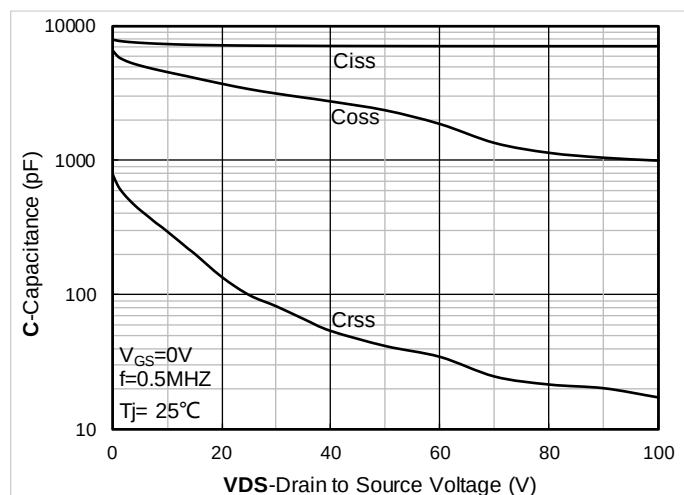


Figure 3. Capacitance Characteristics; typical values

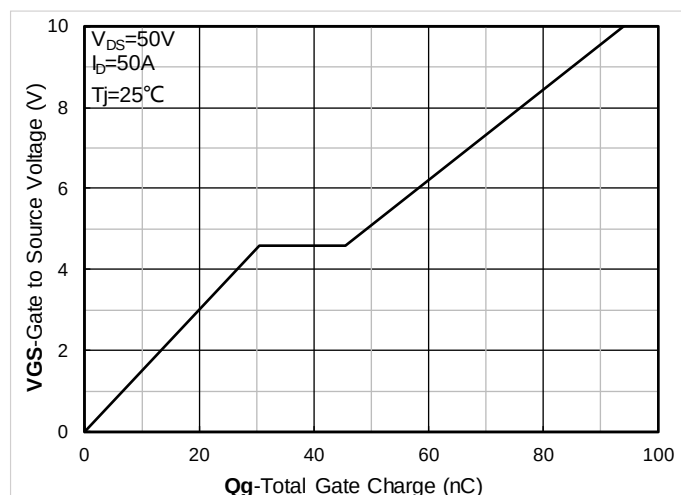


Figure 4. Gate Charge; typical values

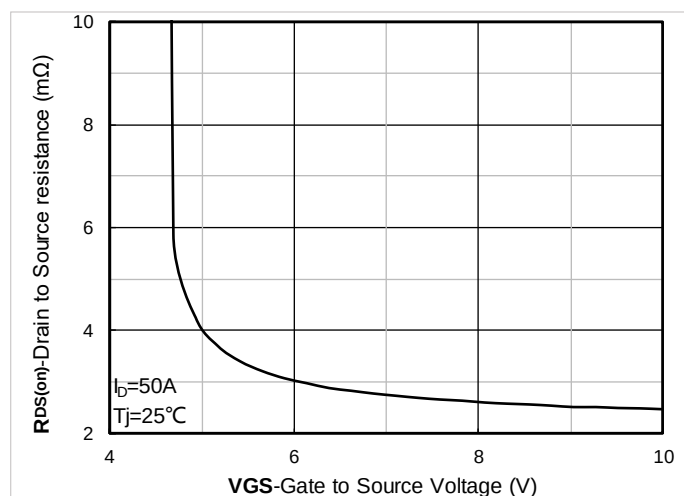


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

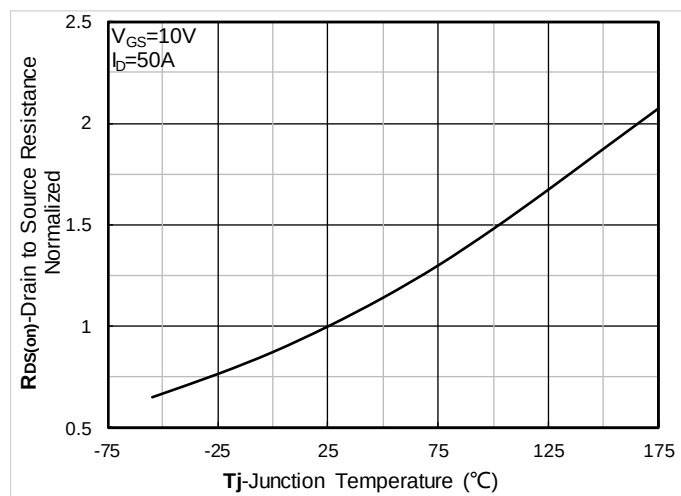


Figure 6. Normalized On-Resistance

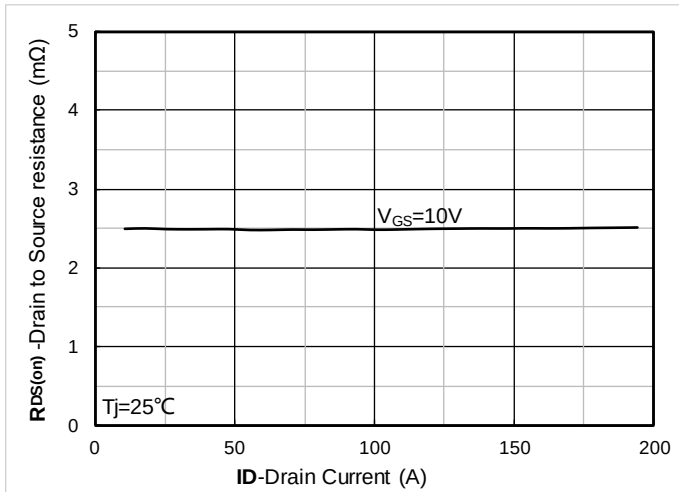


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

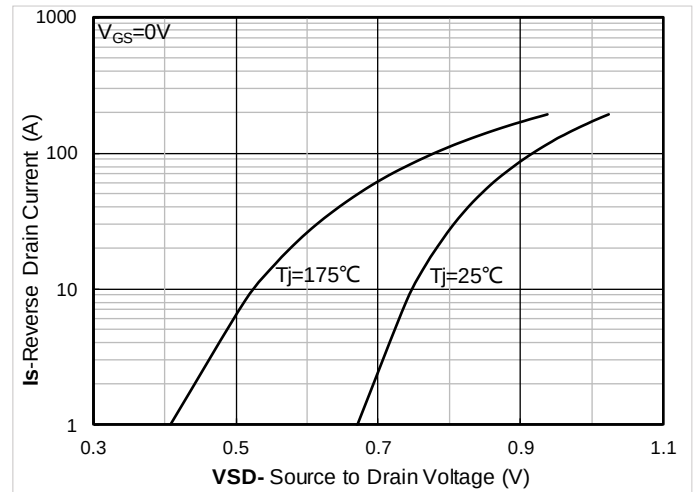


Figure 8. Forward characteristics of reverse diode; typical values

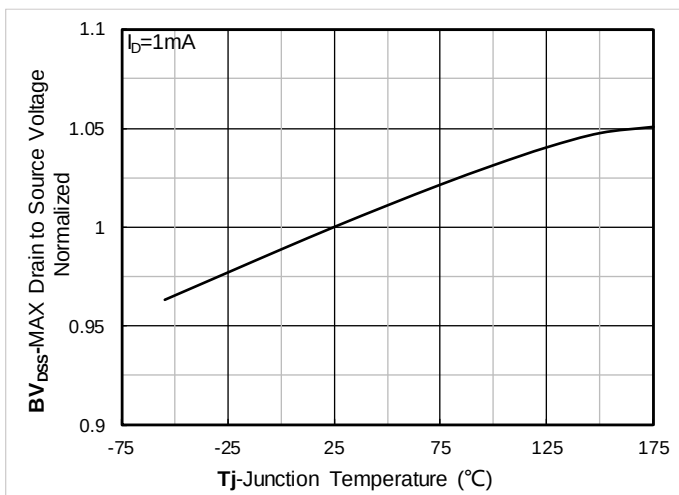


Figure 9. Normalized breakdown voltage

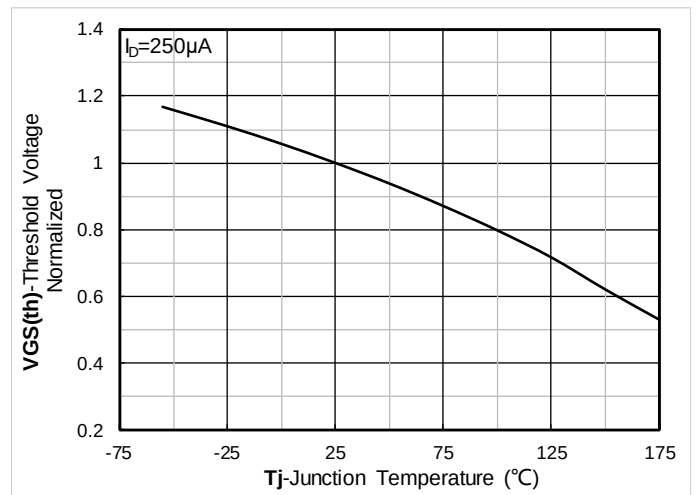


Figure 10. Normalized Threshold voltage

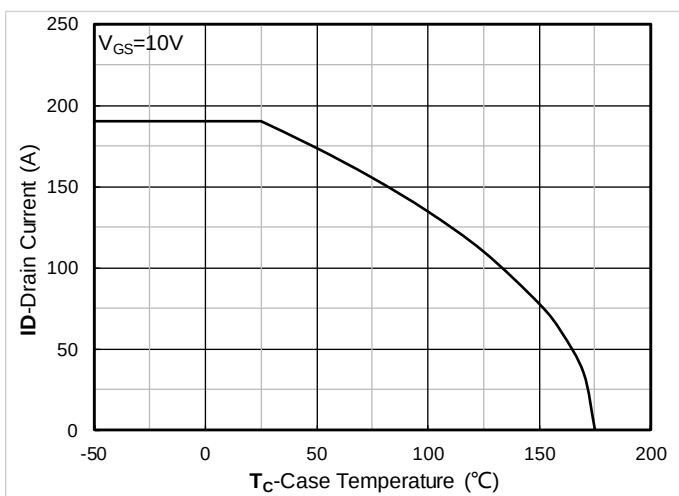


Figure 11. Current dissipation

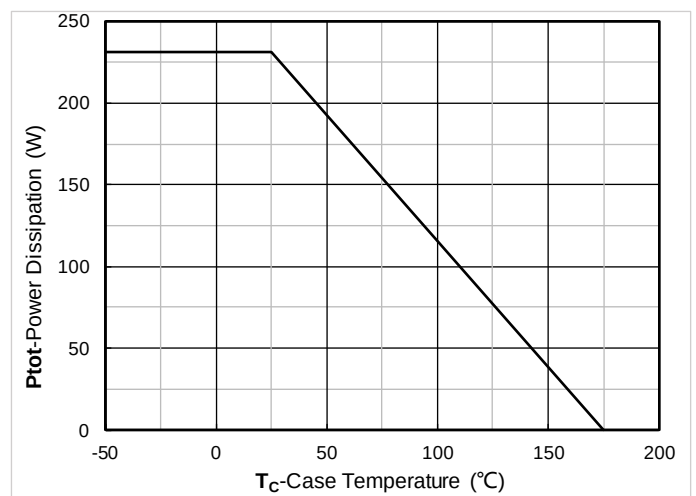


Figure 12. Power dissipation

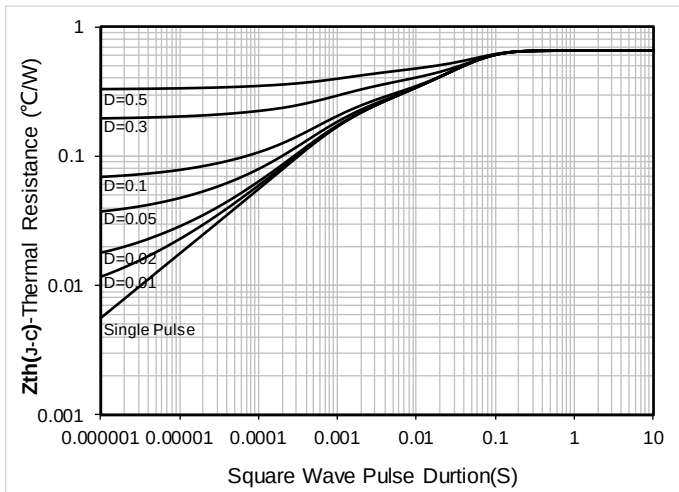


Figure 13. Maximum Transient Thermal Impedance

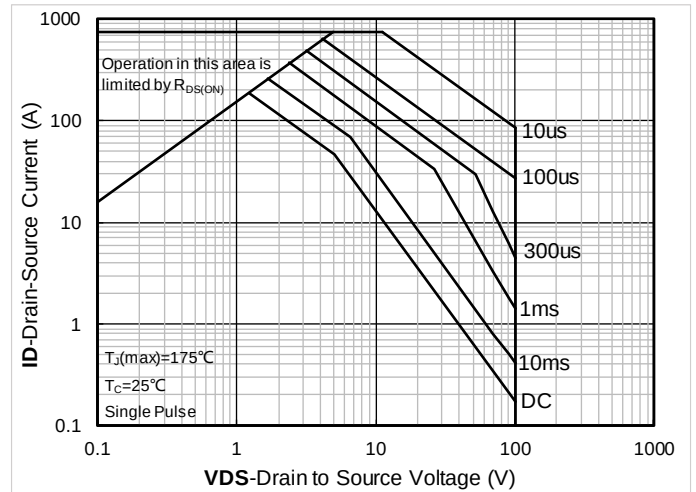
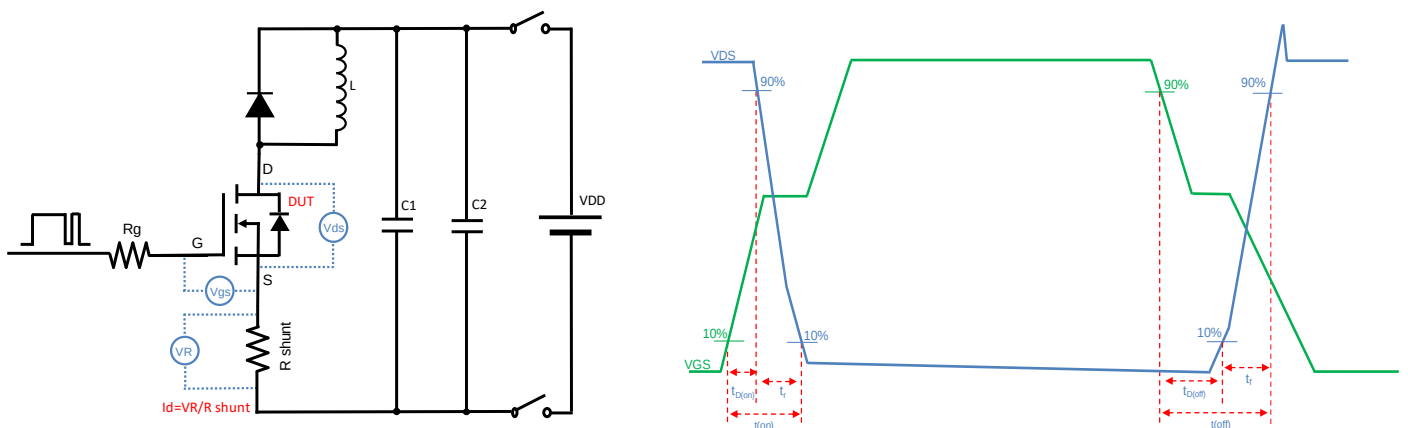
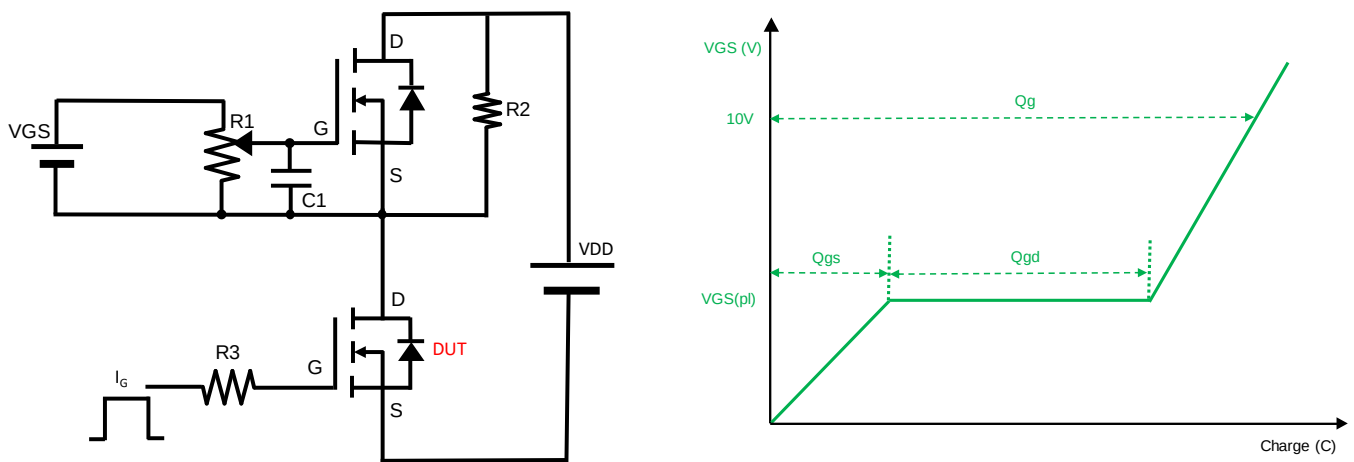
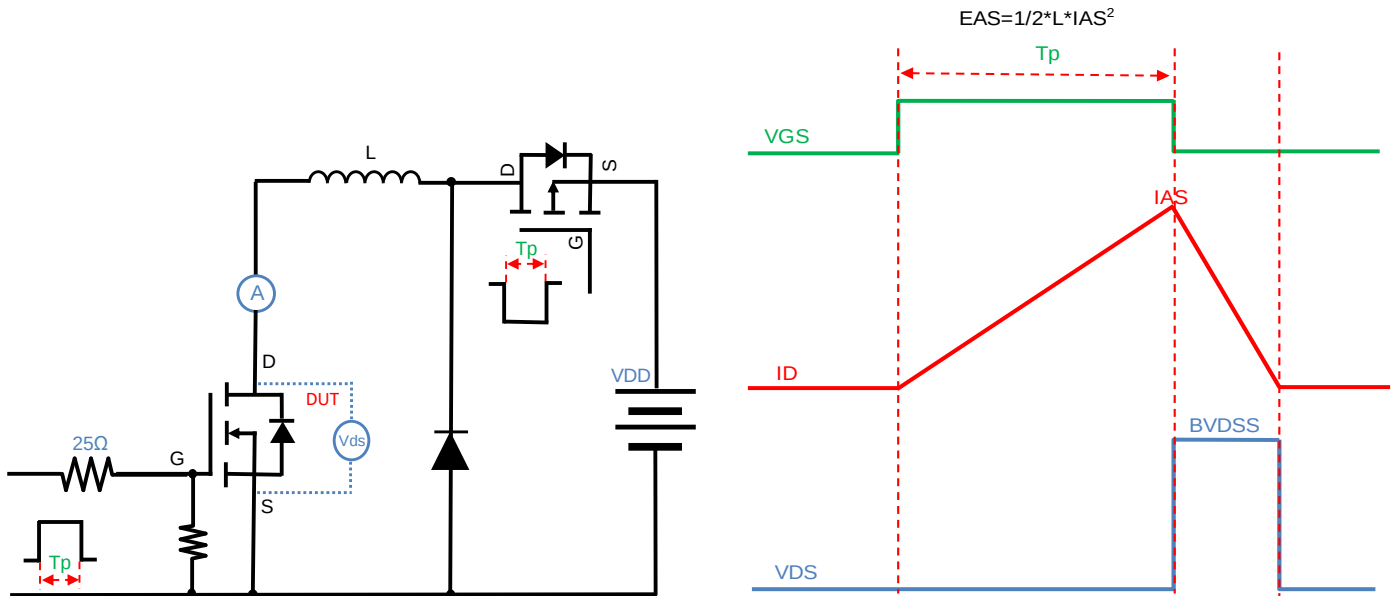


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms



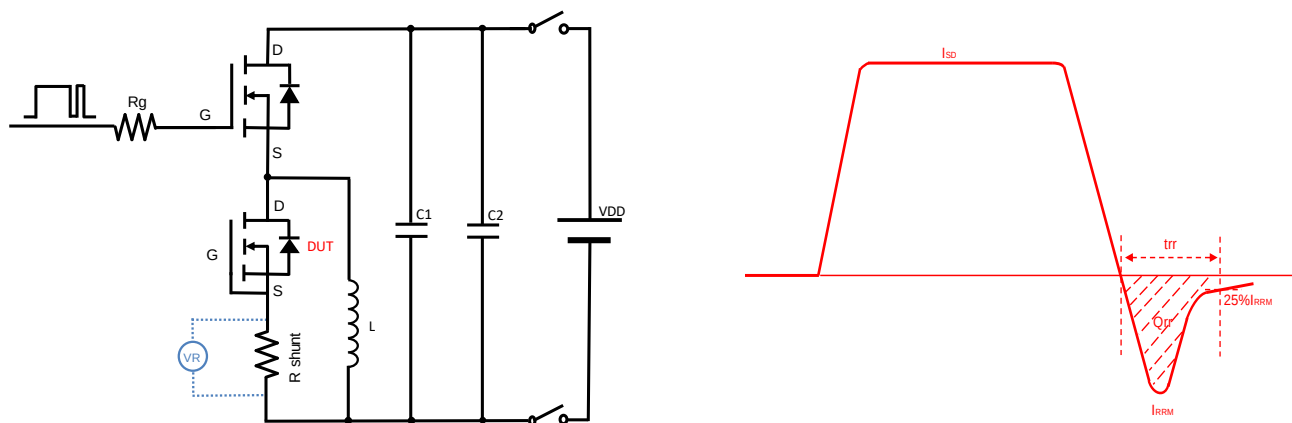
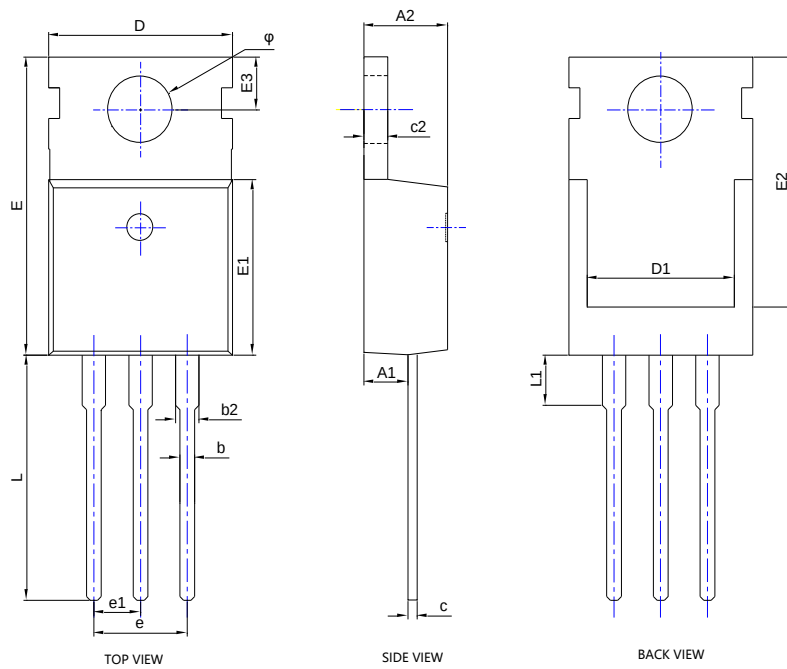


Figure D. Diode Recovery Test Circuit & Waveform

■ TO-220AB-E Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.093	0.114	2.350	2.900
A2	0.176	0.184	4.470	4.670
b	0.028	0.036	0.710	0.910
b2	0.048	0.054	1.220	1.360
c	0.019	0.024	0.470	0.600
c2	0.047	0.055	1.200	1.400
D	0.382	0.408	9.700	10.370
D1	0.276	0.350	7.000	8.890
E	0.579	0.622	14.700	15.800
E1	0.350	0.373	8.900	9.470
E2	0.463	0.535	11.750	13.600
E3	0.108BSC		2.740BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.508	0.583	12.900	14.800
L1	0.100	0.151	2.540	3.840
φ	0.142	0.154	3.600	3.900

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

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