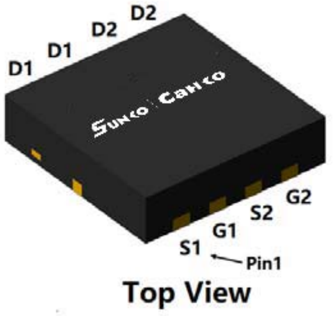
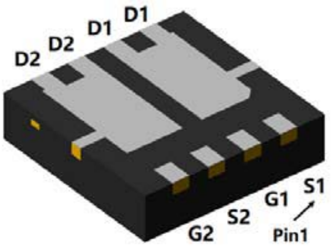
N-Channel and P-Channel Complementary MOSFET

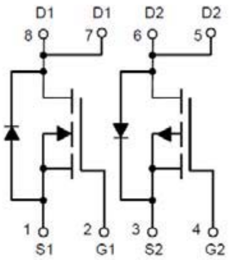


Top View



Bottom View

DFN3333-8L



Product Summary

NMOS

● V_{DS}	40V
● I_D	24A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜16mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	＜21mΩ

PMOS

● V_{DS}	-40V
● I_D	-18A
● $R_{DS(ON)}$(at V_{GS}=-10V)	＜29mΩ
● $R_{DS(ON)}$(at V_{GS}=-4.5V)	＜41mΩ

- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Wireless charger
- Load switching
- Power management

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	40	-40	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃	I_D	7	-5	A
	T_A=100℃		4	-3	
	T_C=25℃		24	-18	
	T_C =100℃		15	-11	
Pulsed Drain Current ^{A}		I_{DM}	96	-72	A
Avalanche energy ^{B}		EAS	6.25	6.25	mJ
Total Power Dissipation ^{C}	T_A=25℃	P_D	1.6	1.6	W
	T_A=100℃		0.6	0.6	
	T_C=25℃		18.9	19.5	
	T_C =100℃		7.5	7.8	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient	Steady-State	$R_{\theta JA}$	60	75	60	75	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	5.5	6.6	5.3	6.4	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCQ016NP04A	F1	Q016NP04A	5000	10000	100000	13'' reel

■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A	-	11.5	16	mΩ
		V_{GS}=4.5V, I_D=8A	-	15	21	
Diode Forward Voltage	V_{SD}	I_S=15A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	24	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=1MHz	-	965	-	pF
Output Capacitance	C_{oss}		-	96	-	
Reverse Transfer Capacitance	C_{rss}		-	85	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=20V,I_D=15A	-	21.4	-	nC
Gate-Source Charge	Q_{gs}		-	3.4	-	
Gate-Drain Charge	Q_{gd}		-	5	-	
Reverse Recovery Charge	Q_{rr}	I_F=15A, di/dt=100A/us	-	6.3	-	nC
Reverse Recovery Time	t_{rr}		-	11.7	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=20V, I_D=15A R_{GEN}=2.2Ω	-	7.8	-	ns
Turn-on Rise Time	t_r		-	143	-	
Turn-off Delay Time	$t_{D(off)}$		-	25.6	-	
Turn-off fall Time	t_f		-	5.2	-	

■ PMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-40V, V_{GS}=0V, Tj=150℃	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.1	-1.6	-2.1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-15A	-	22	29	mΩ
		V_{GS}=-4.5V, I_D=-8A	-	30	41	
Diode Forward Voltage	V_{SD}	I_S=-15A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	16	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-18	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-20V, V_{GS}=0V, f=1MHz	-	1225	-	pF
Output Capacitance	C_{oss}		-	120	-	
Reverse Transfer Capacitance	C_{rss}		-	110	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-20V, I_D=-15A	-	27	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Reverse Recovery Charge	Q_{rr}	I_F=-15A, di/dt=100A/us	-	20	-	nC
Reverse Recovery Time	t_{rr}		-	21	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-20V, ID=-15A R_{GEN}=2.2Ω	-	7.7	-	ns
Turn-on Rise Time	t_r		-	106.7	-	
Turn-off Delay Time	$t_{D(off)}$		-	68.3	-	
Turn-off fall Time	t_f		-	37.6	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. NMOS: T_J=25℃, V_{GS}=10V, R_G=25Ω, L=0.5mH, IAS=5A.
PMOS: T_J=25℃, V_{GS}=-10V, R_G=25Ω, L=0.5mH, IAS=-5A.

C. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

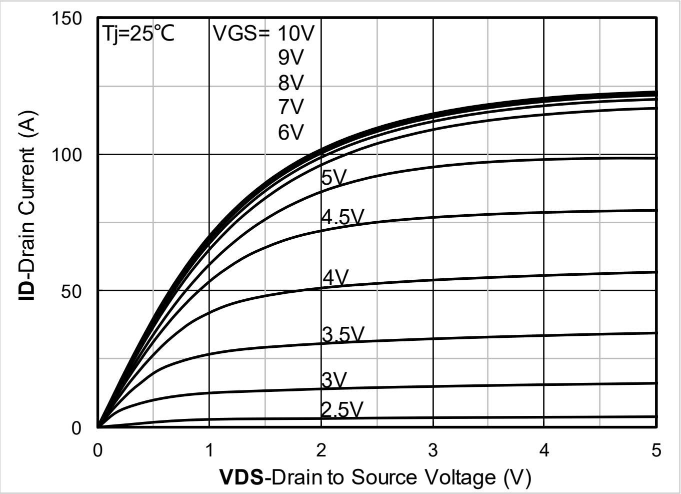


Figure 1. Output Characteristics

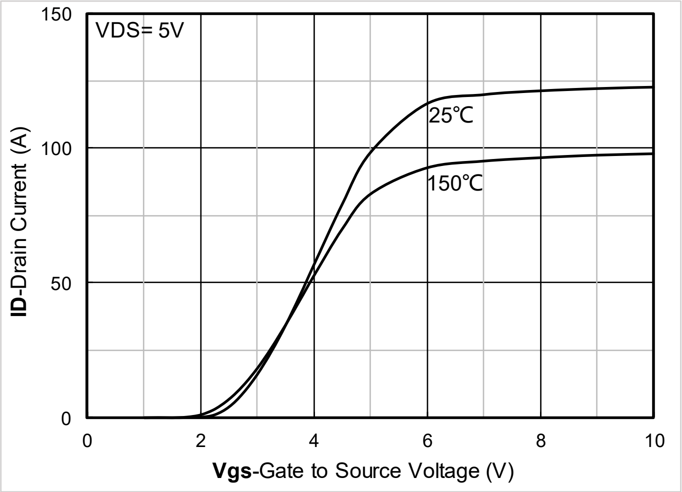


Figure 2. Transfer Characteristics

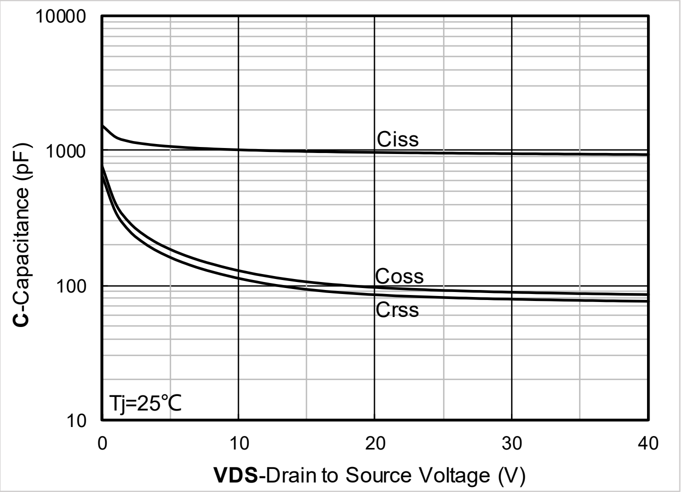


Figure 3. Capacitance Characteristics

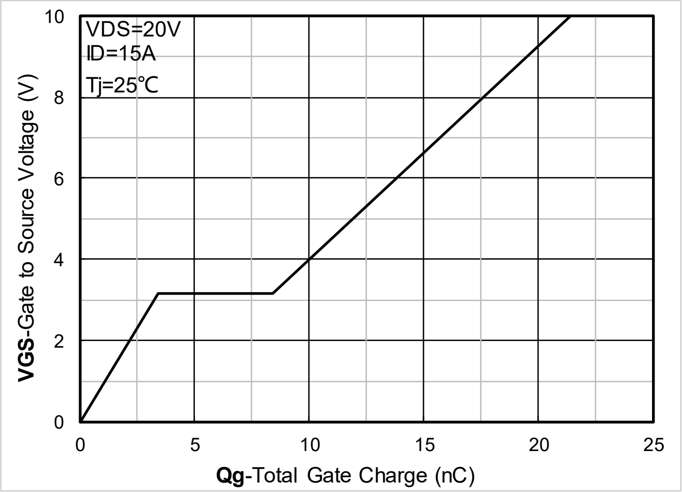


Figure 4. Gate Charge

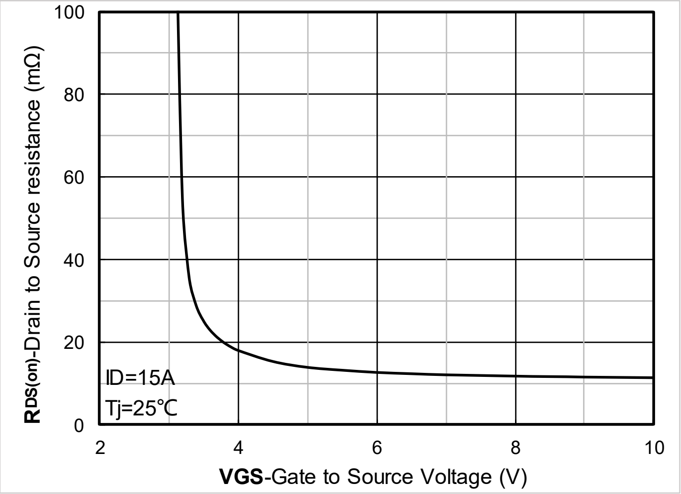


Figure 5. On-Resistance VS Gate to Source Voltage

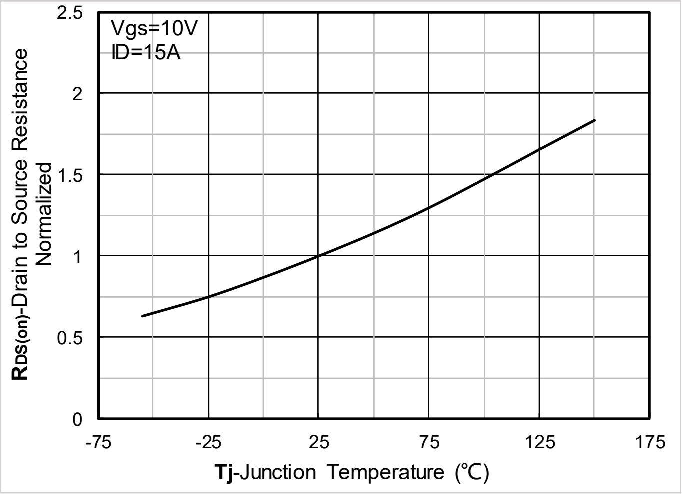


Figure 6. Normalized On- Resistance

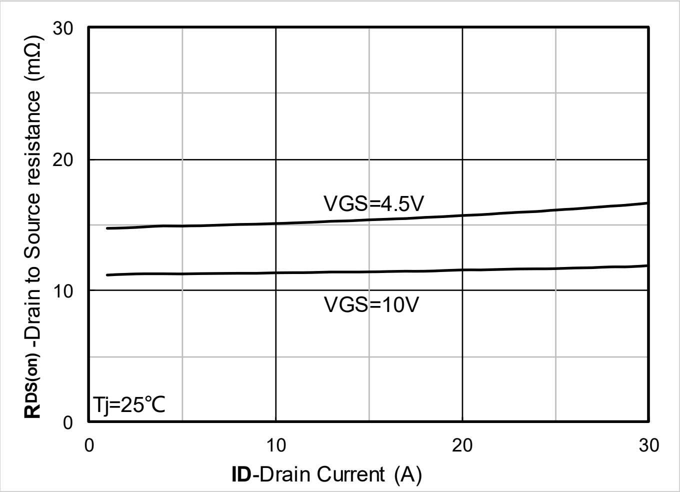


Figure 7. RDS(on) VS Drain Current

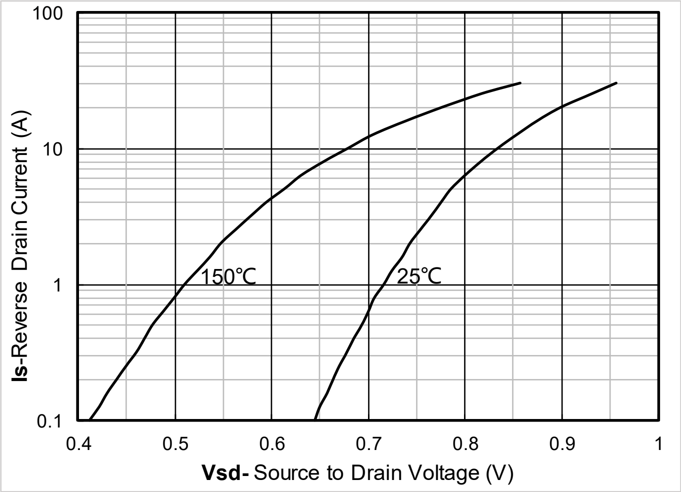


Figure 8. Forward characteristics of reverse diode

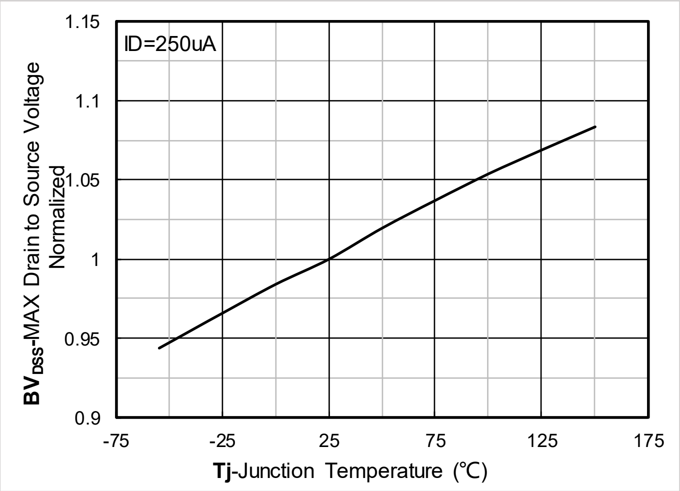


Figure 9. Normalized breakdown voltage

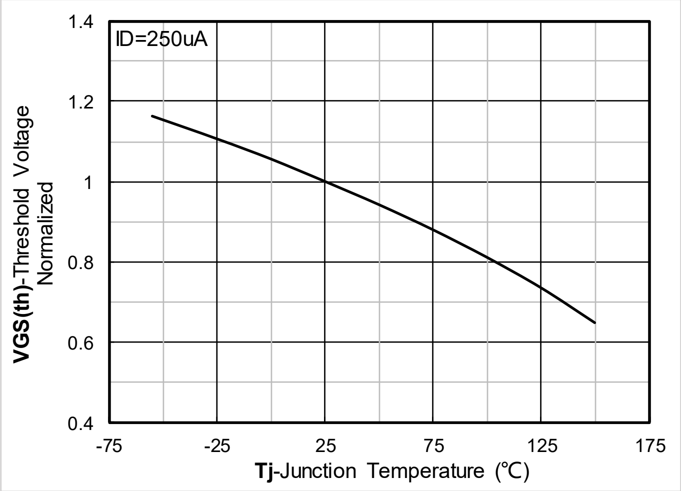


Figure 10. Normalized Threshold voltage

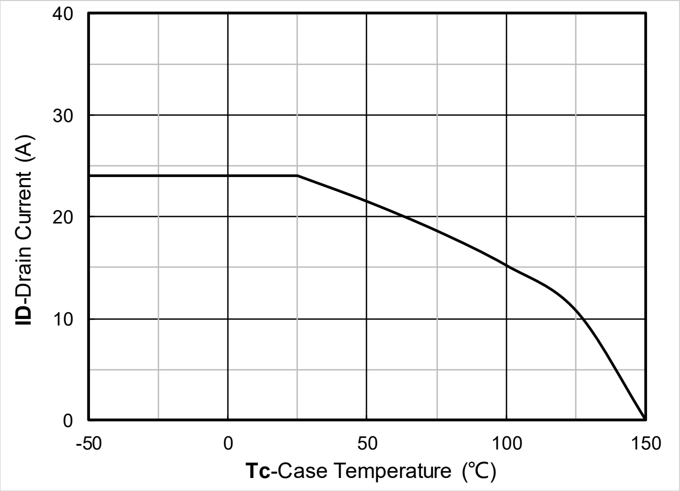


Figure 11. Current dissipation

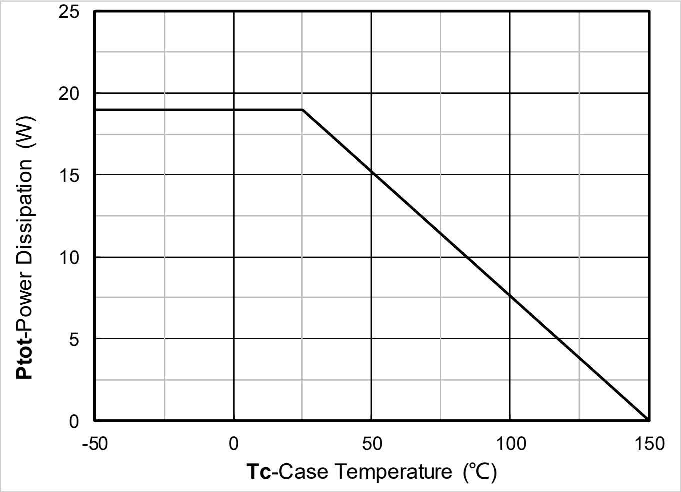


Figure 12. Power dissipation

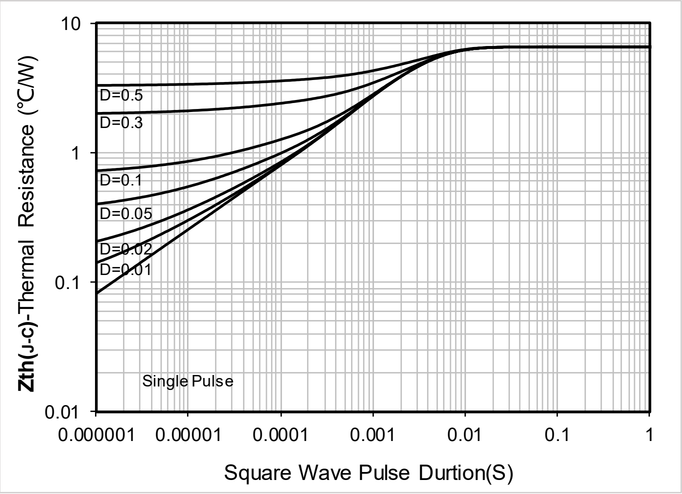


Figure 13. Maximum Transient Thermal Impedance

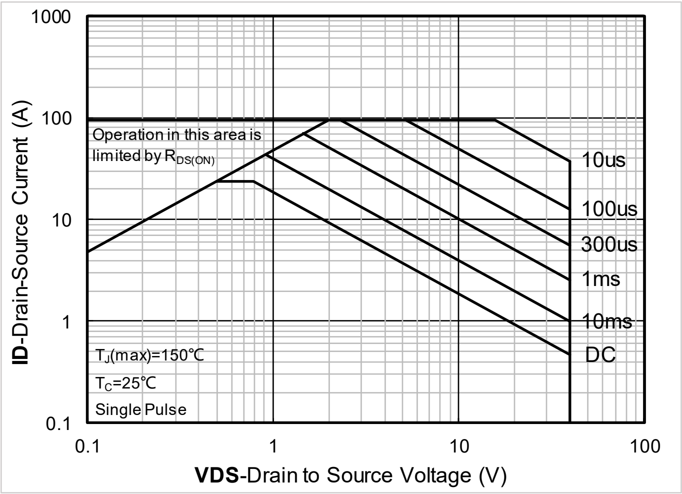


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

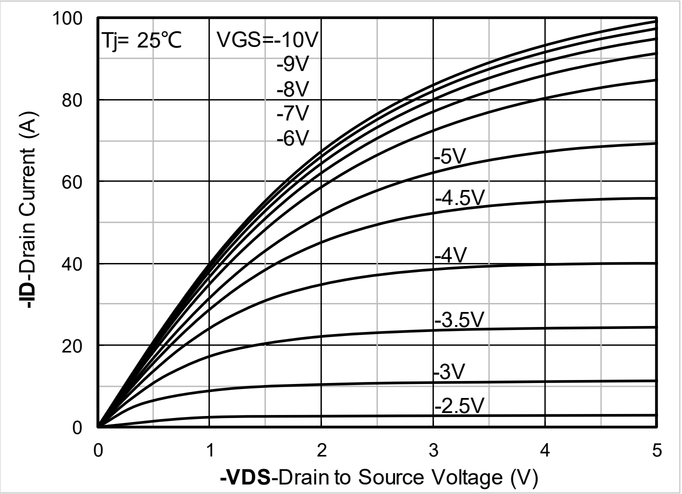


Figure 1. Output Characteristics

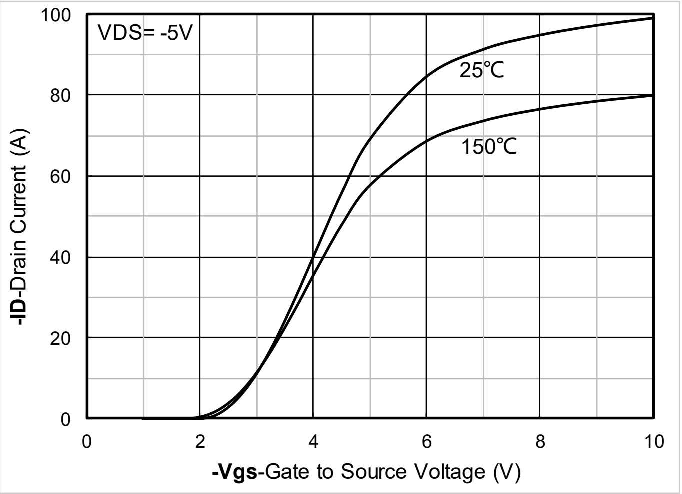


Figure 2. Transfer Characteristics

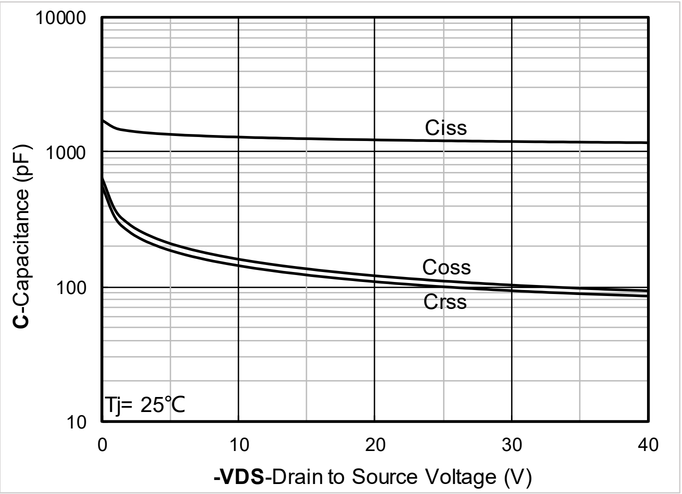


Figure 3. Capacitance Characteristics

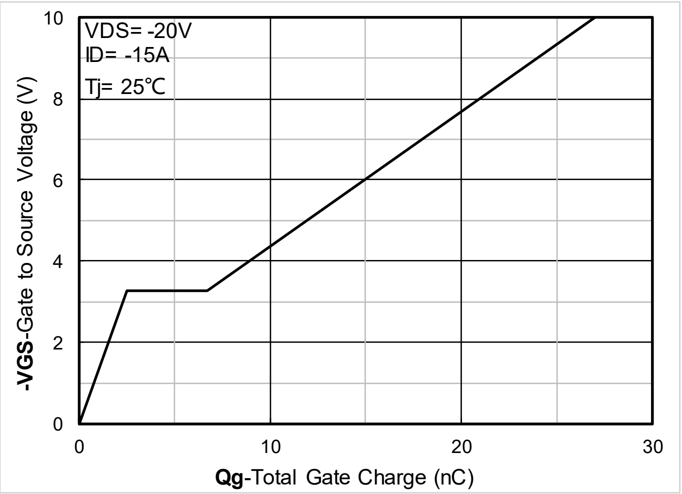


Figure 4. Gate Charge

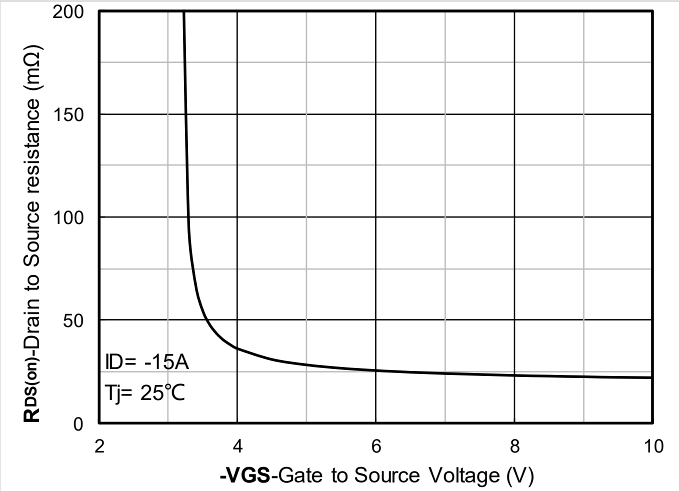


Figure 5. On-Resistance vs Gate to Source Voltage

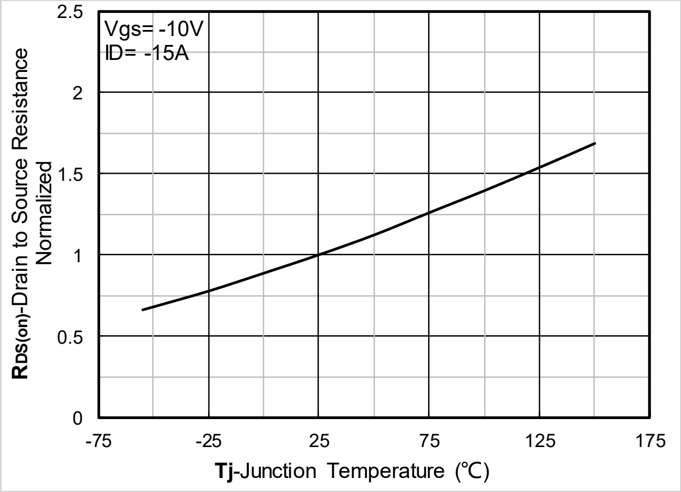


Figure 6. Normalized On-Resistance

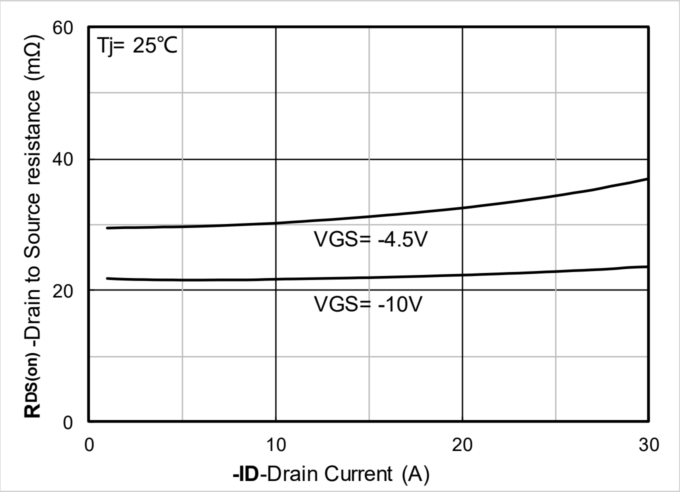


Figure 7. $R_{DS(on)}$ VS Drain Current

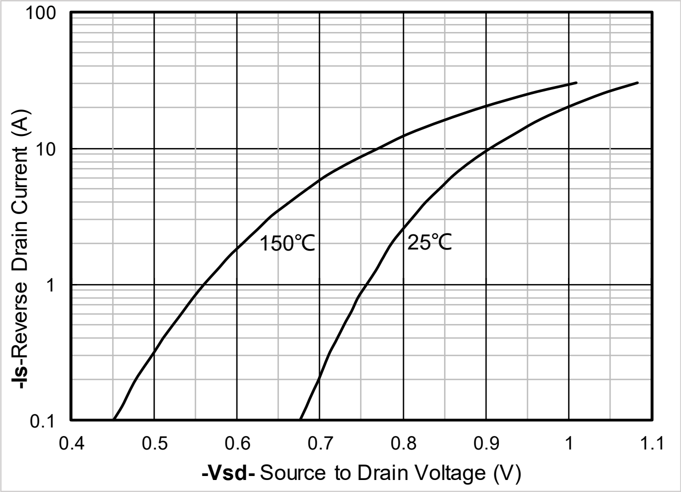


Figure 8. Forward characteristics of reverse diode

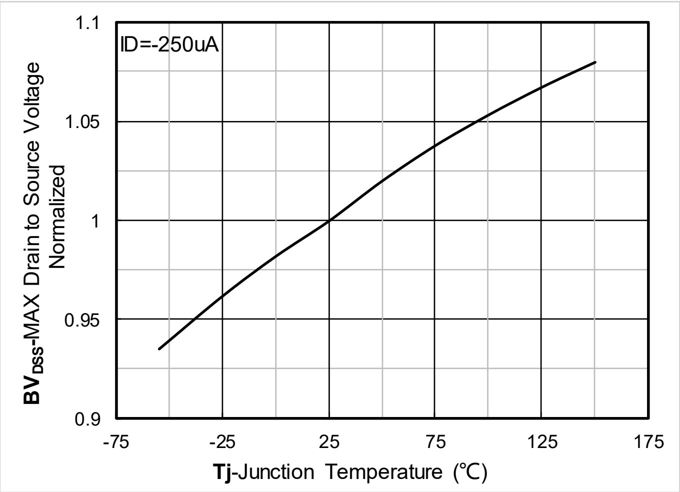


Figure 9. Normalized breakdown voltage

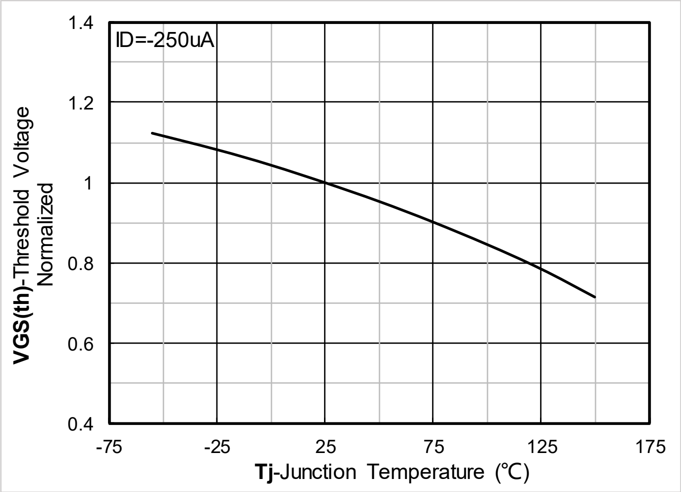


Figure 10. Normalized Threshold voltage

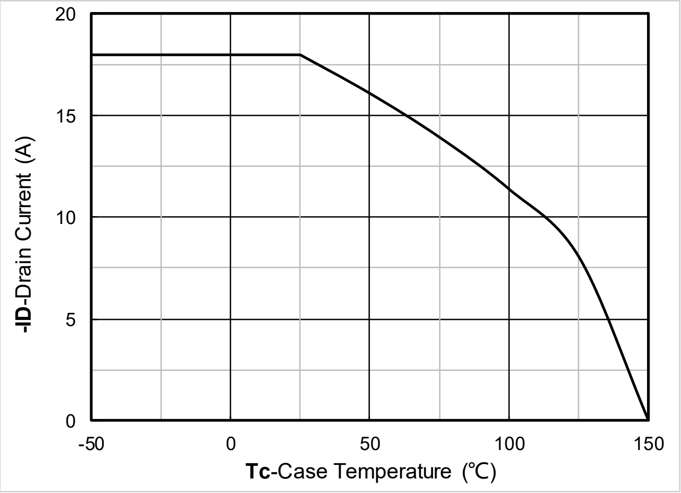


Figure 11. Current dissipation

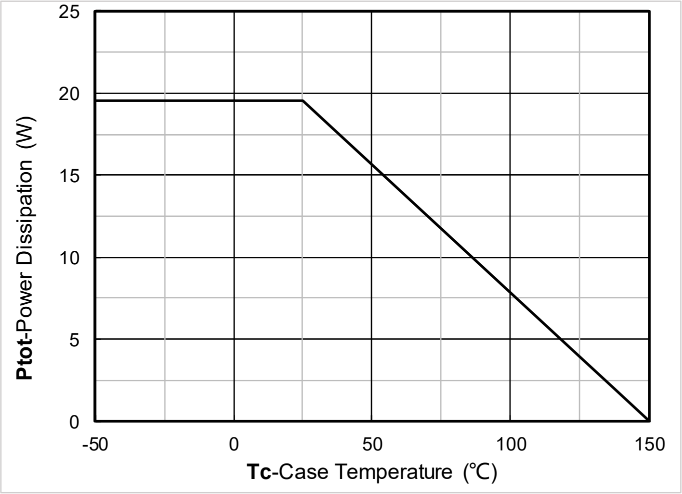


Figure 12. Power dissipation

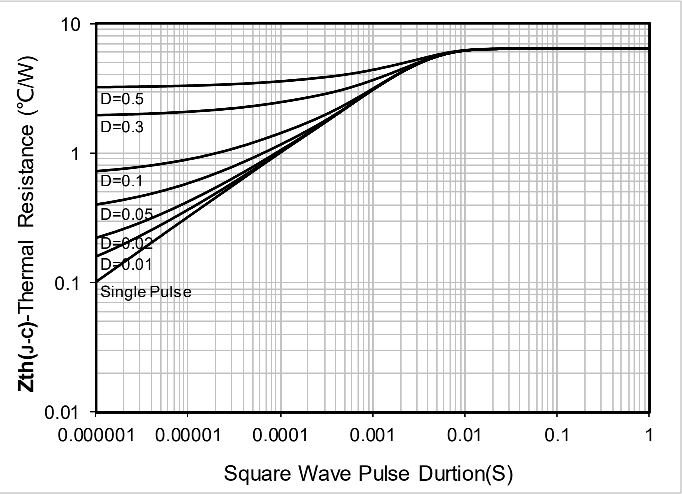


Figure 13. Maximum Transient Thermal Impedance

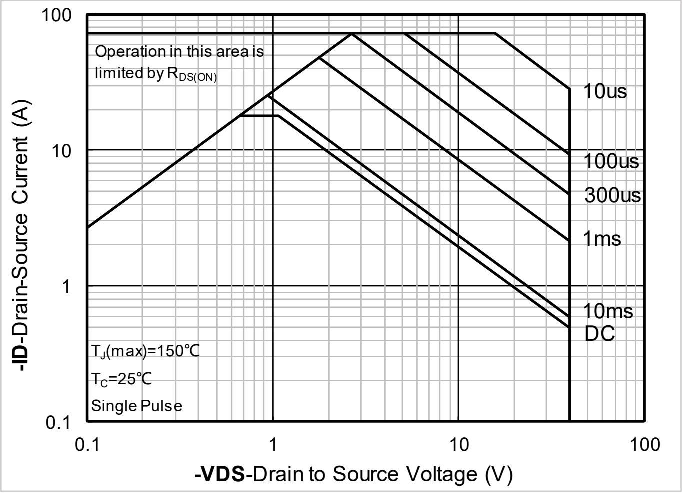
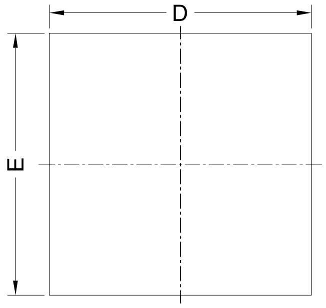
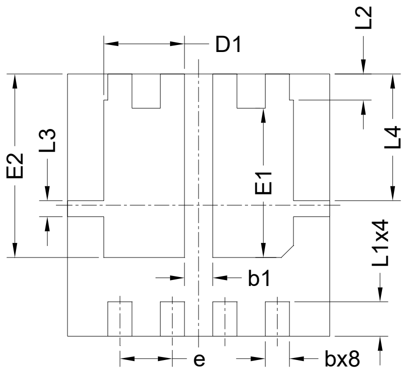


Figure 14. Safe Operation Area

■ DFN3333-8L-B-0.8MM Package information

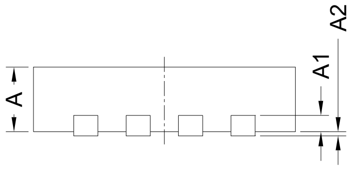


Top View
正面视图

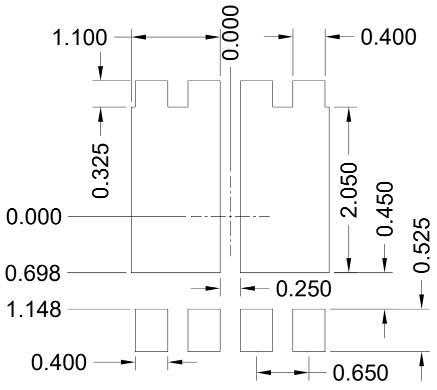


Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
E2	2.175	2.275	2.375
L1	0.325	0.425	0.525
L2	0.325 BSC		
L3	0.200 BSC		
L4	1.570 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		
b1	0.35 REF		



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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