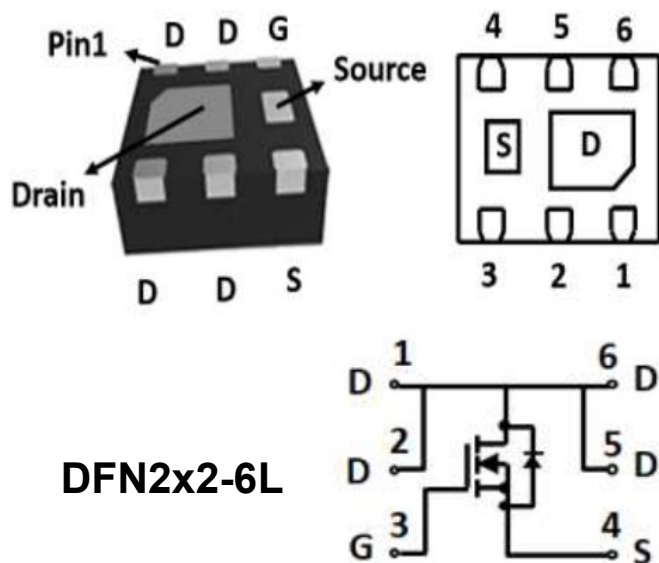


N-Channel Enhancement Mode Field Effect Transistor



DFN2x2-6L

Product Summary

- V_{DS} 20V
- I_D 12A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 13mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) < 16mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) < 25mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High Power and current handling capability

Applications

- PWM application
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A=25^\circ C$	I_D	12	A
	$T_A=70^\circ C$		9.6	
Pulsed Drain Current ^A		I_{DM}	50	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=70^\circ C$		1.6	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	50	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCQ2012A	F1	N2012A	3000	30000	120000	7" reel

■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS1}	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=5A$		10	13	m Ω
		$V_{GS}=2.5V, I_D=3A$		12.5	16	
		$V_{GS}=1.8V, I_D=2A$		17	25	
Diode Forward Voltage	V_{SD}	$I_S=5A, V_{GS}=0V$			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		777		pF
Output Capacitance	C_{oss}			164		
Reverse Transfer Capacitance	C_{rss}			140		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=4.5V, V_{DS}=10V, I_D=5.6A$		25.5		nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			4.6		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DS}=10V, R_L=1.5\Omega$ $R_{GEN}=3\Omega$		4.4		
Turn-on Rise Time	t_r			28.2		
Turn-off Delay Time	$t_{D(off)}$			16.2		
Turn-off fall Time	t_f			26		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

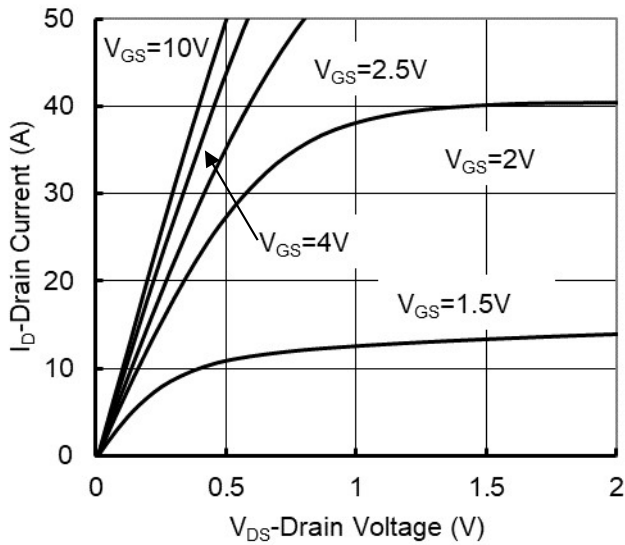


Figure1. Output Characteristics

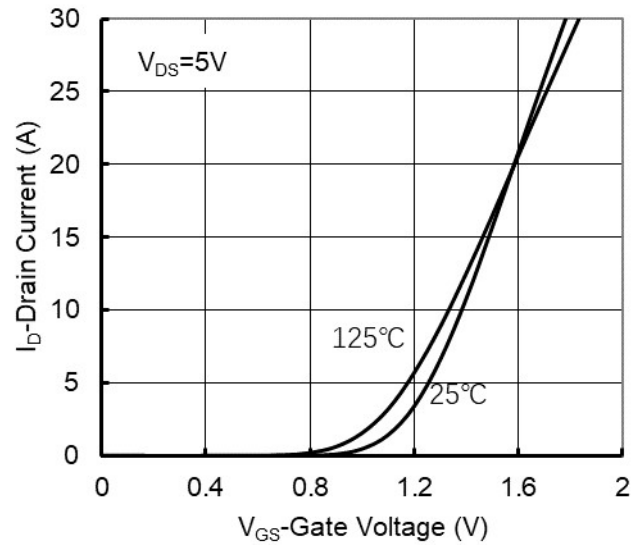


Figure2. Transfer Characteristics

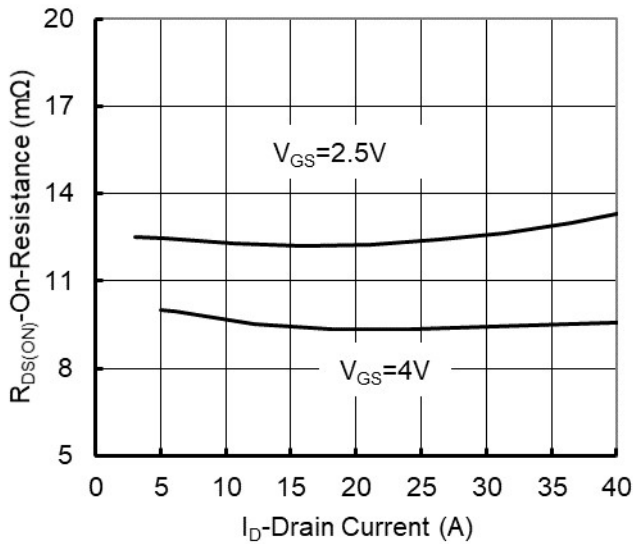


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

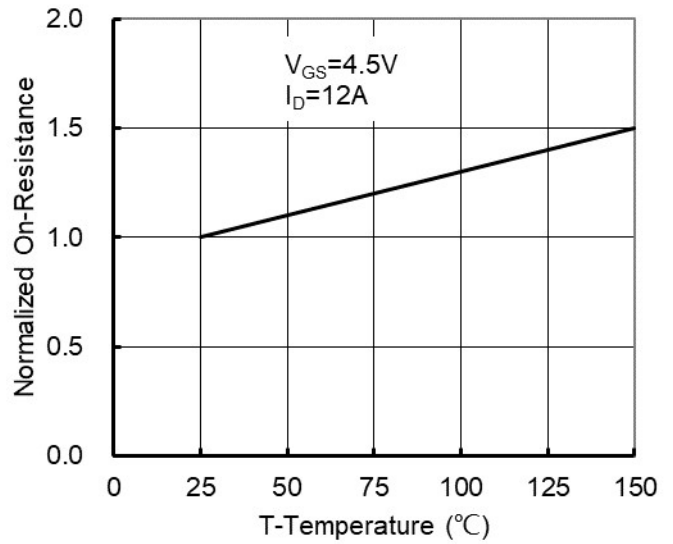


Figure 4: On-Resistance vs. Junction Temperature

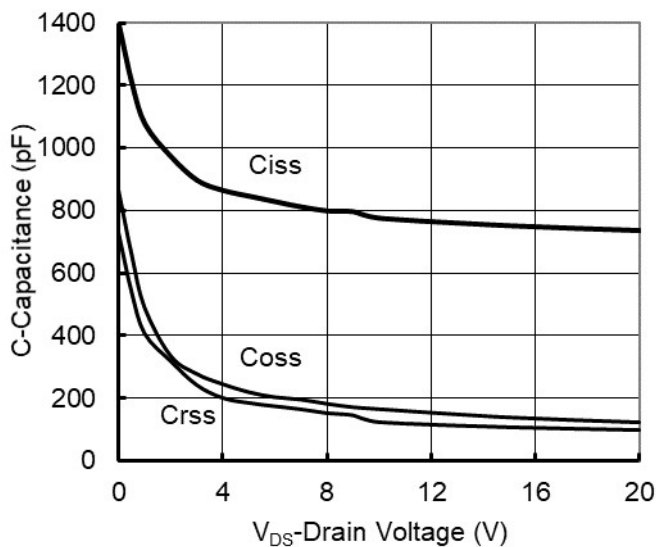


Figure5. Capacitance Characteristics

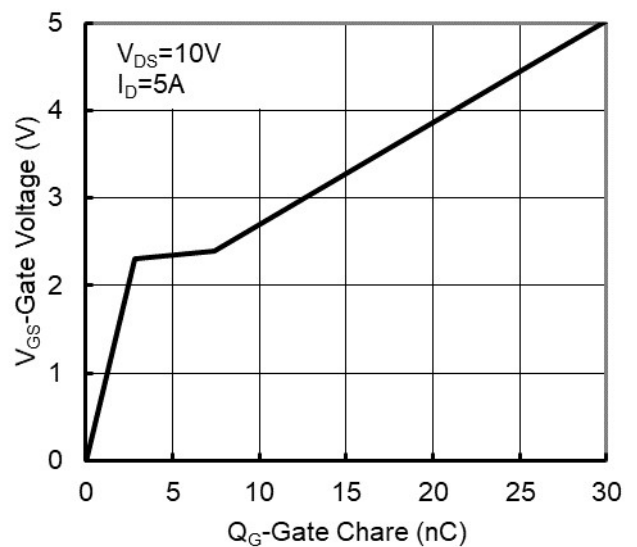


Figure6. Gate Charge

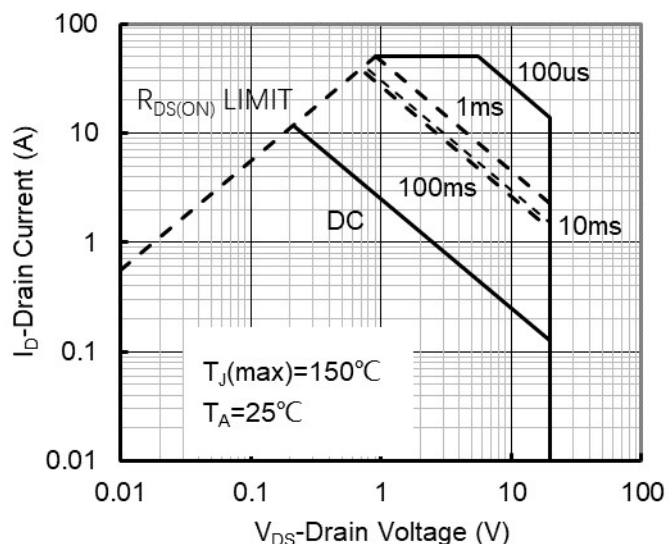


Figure7. Safe Operation Area

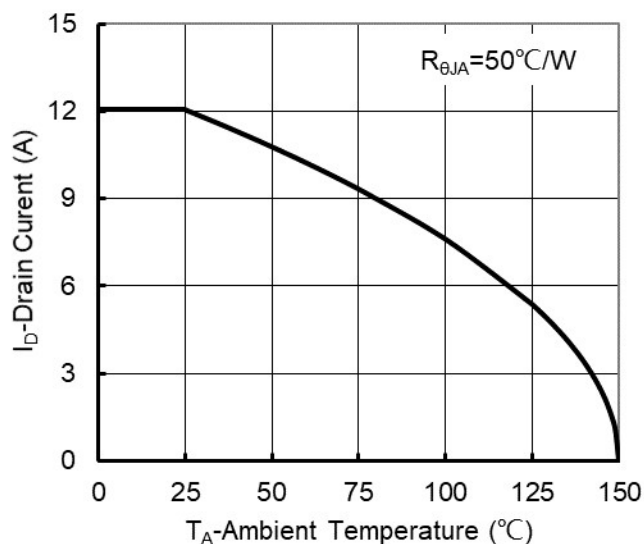


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

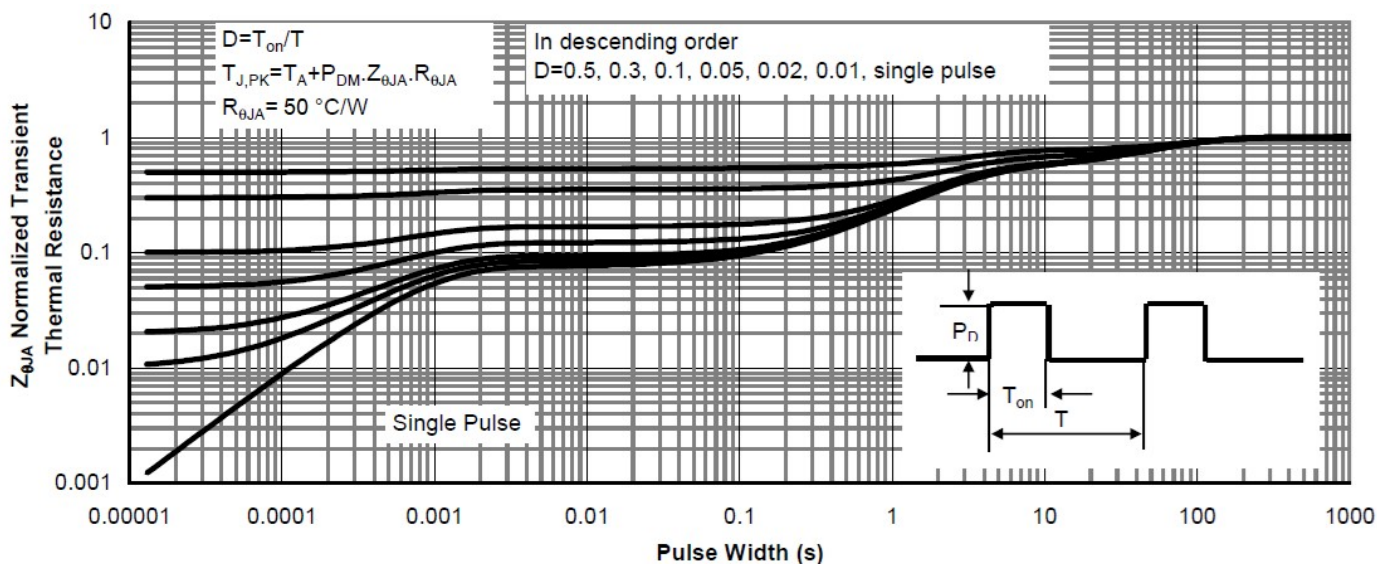
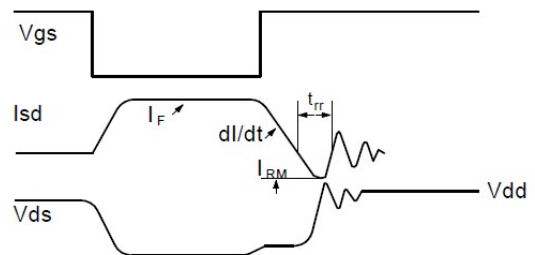


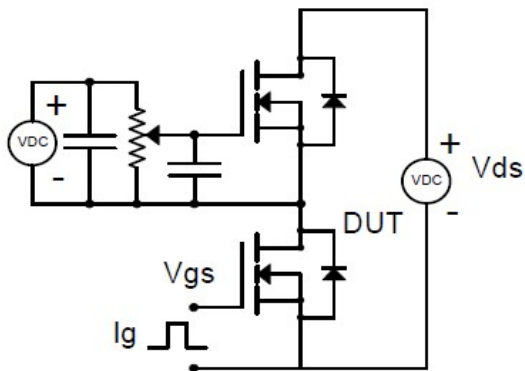
Figure9. Normalized Maximum Transient Thermal Impedance



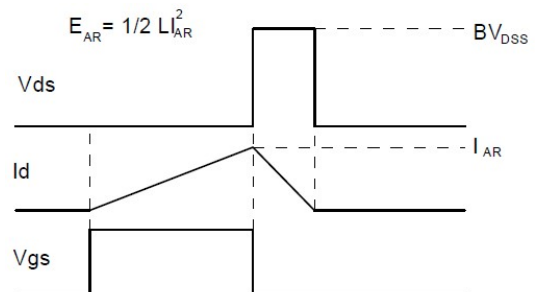
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

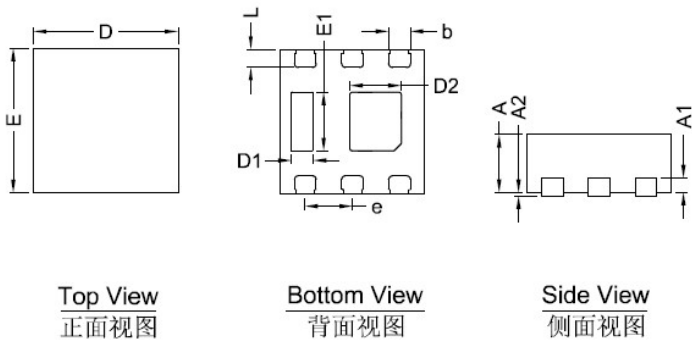


Gate Charge Test Circuit & Waveform



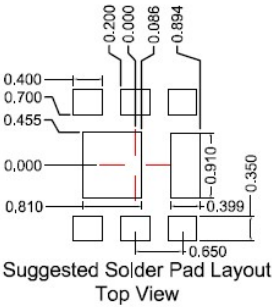
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ DFN2x2-6L Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		

Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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