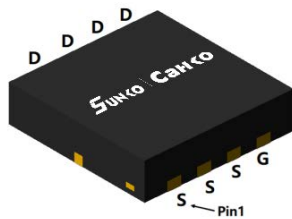
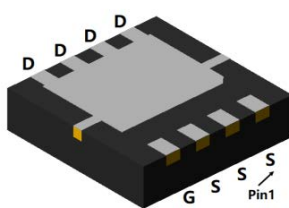


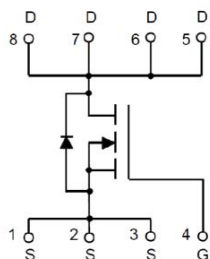
P-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



DFN3333-8L

Product Summary

- V_{DS} -60V
- I_D -22.5A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <47 m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <60 m Ω
- 100% EAS Tested

General Description

- Split gate trench MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Low C_{rss}
- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Industrial DC/DC Conversion Circuits

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	-22.5	A
	$T_C=100^\circ\text{C}$		-14.3	
Pulsed Drain Current ^A		I_{DM}	-90	A
Avalanche energy ^B		E_{AS}	81	mJ
Total Power Dissipation ^C	$T_C=25^\circ\text{C}$	P_D	43	W
	$T_C=100^\circ\text{C}$		17.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCQ23GP06A	F1	Q23GP06A	5000	10000	100000	13" reel

SCQ23GP06A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA		-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V,V _{GS} =0V	T _J =25℃			-1	μA
			T _J =55℃			-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V				±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA		-1.3	-1.8	-2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D =-20A			35	47	mΩ
		V _{GS} = -4.5V, I _D =-10A			45	60	
Gate Resistance	R _g	f=1MHz, Open Drain			12		Ω
Diode Forward Voltage	V _{SD}	I _S =-20A,V _{GS} =0V			-0.95	-1.3	V
Maximum Body-Diode Continuous Current	I _S					-23	A
Dynamic Parameters							
Input Capacitance	C _{iss}	V _{DS} =-30V,V _{GS} =0V,f=1MHZ			1100		pF
Output Capacitance	C _{oss}				350		
Reverse Transfer Capacitance	C _{rss}				28		
Switching Parameters							
Total Gate Charge	Q _g (-10V)	V _{GS} =-10V,V _{DS} =-30V,I _D =-20A			18.7		nC
Total Gate Charge	Q _g (-4.5V)				8.8		
Gate-Source Charge	Q _{gs}				4.7		
Gate-Drain Charge	Q _{gd}				3.0		
Reverse Recovery Chrage	Q _{rr}	I _F =-20A, di/dt=100A/us			8.2		ns
Reverse Recovery Time	t _{rr}				20.2		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V,V _{DD} =-30V,R _L =2.5Ω R _{GEN} =6Ω			7.5		
Turn-on Rise Time	t _r				39.5		
Turn-off Delay Time	t _{D(off)}				43.6		
Turn-off fall Time	t _f				55.1		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=0.5mH, I_{AS}=18A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PDSM is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

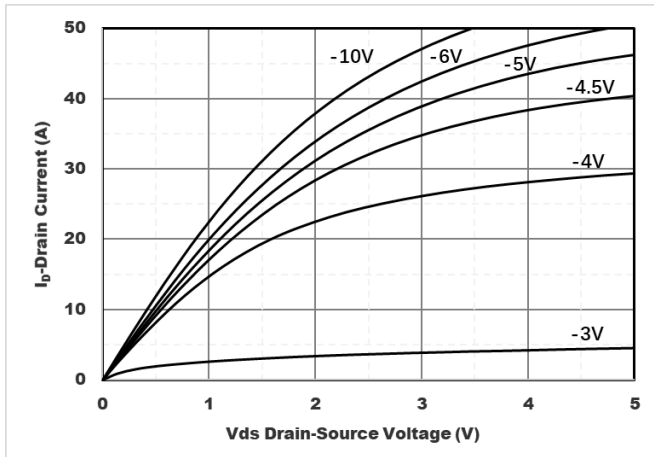


Figure1. Output Characteristics

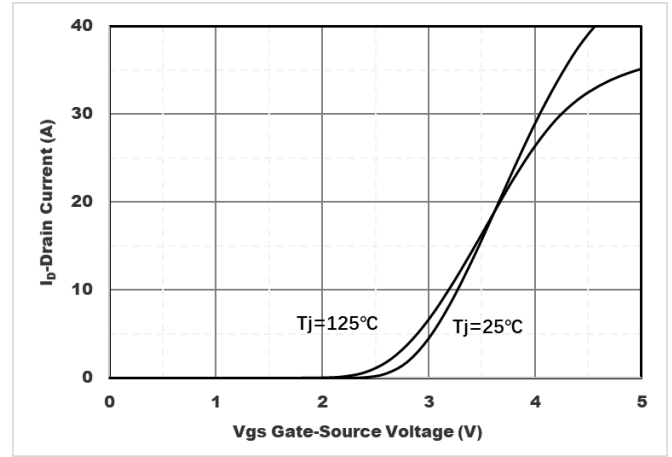


Figure2. Transfer Characteristics

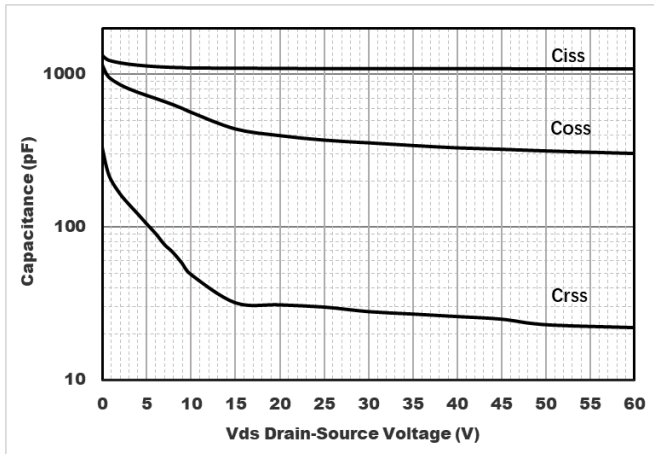


Figure3. Capacitance Characteristics

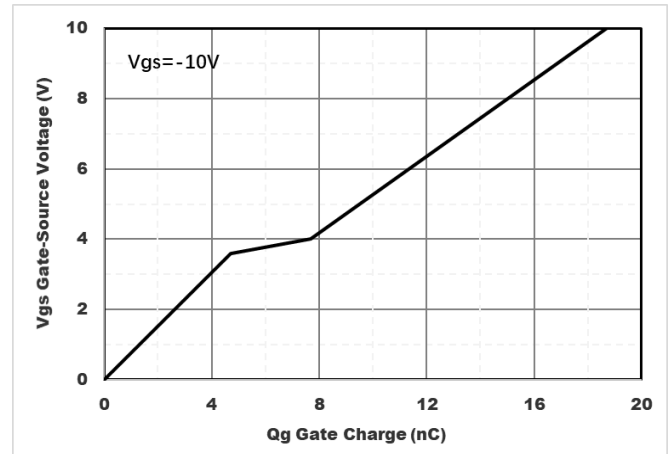


Figure4. Gate Charge

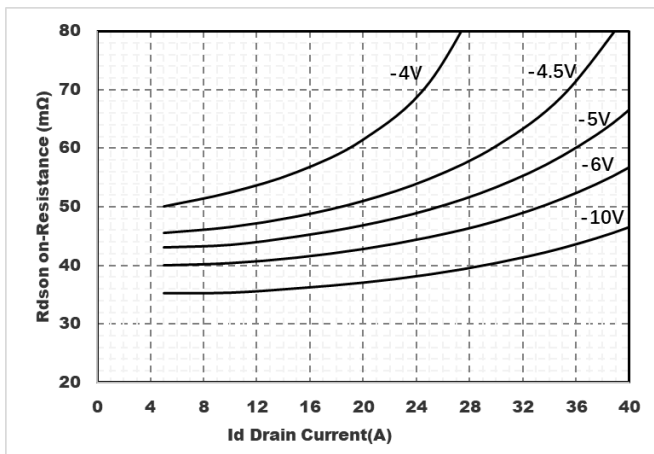


Figure5. : On-Resistance vs. Gate to Source Voltage

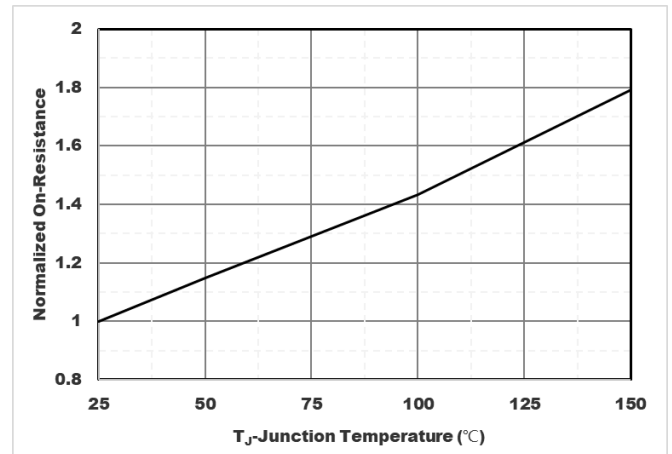


Figure6. Normalized On-Resistance

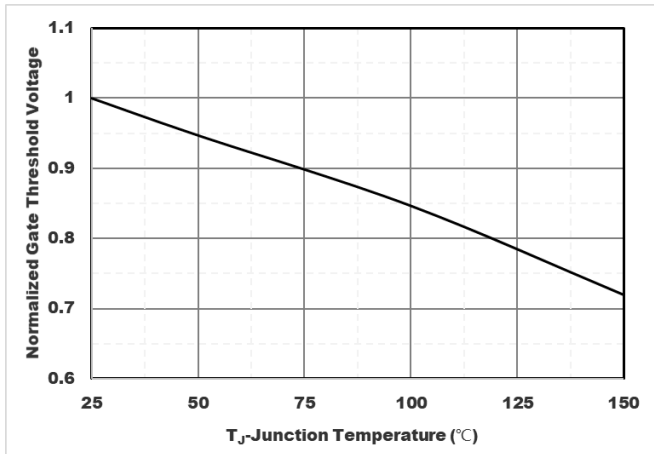


Figure7. Normalized Gate Threshold Voltage

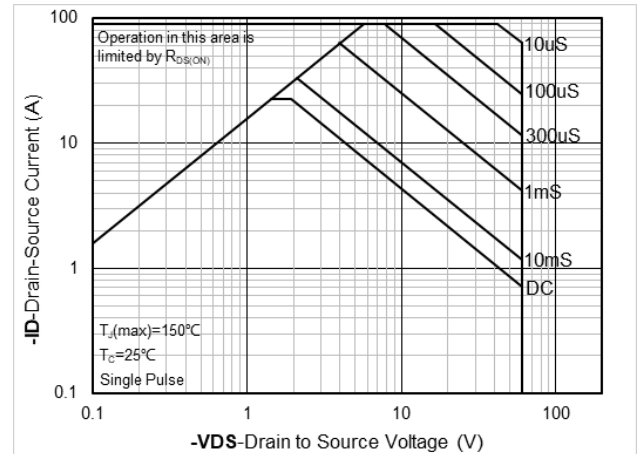


Figure8.Safe Operation Area

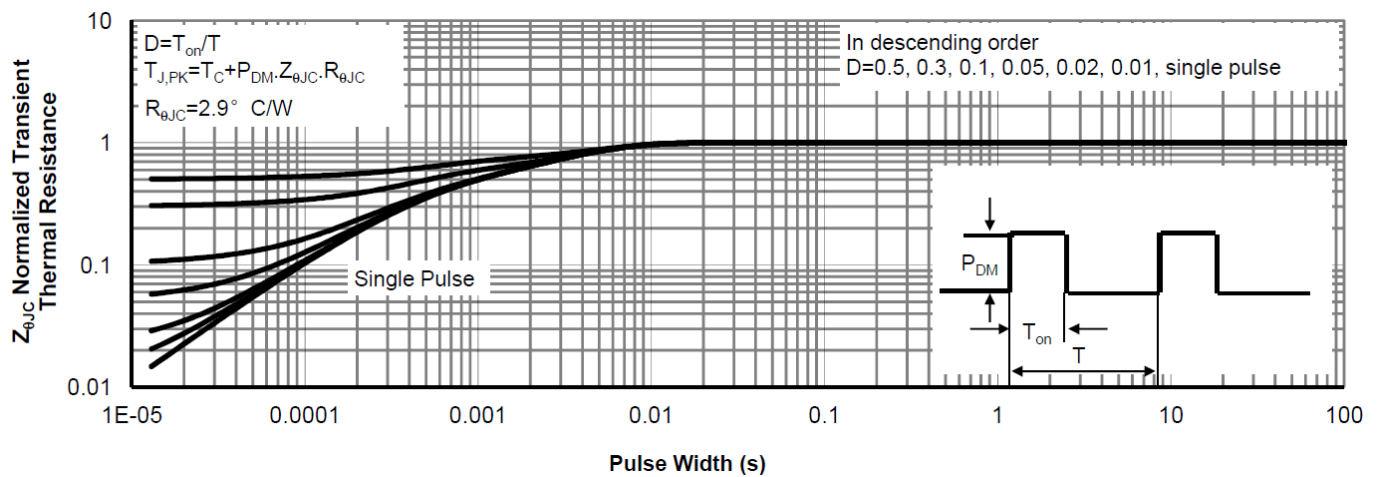
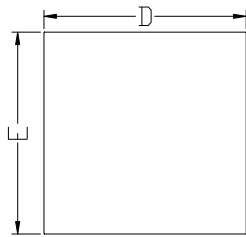
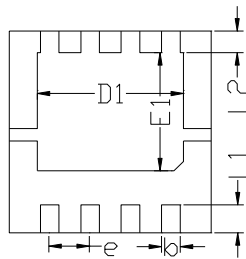


Figure9.Normalized Maximum Transient thermal impedance

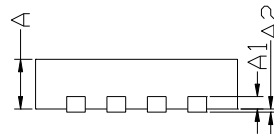
■ DFN3333-8L Package information



Top View
正面视图

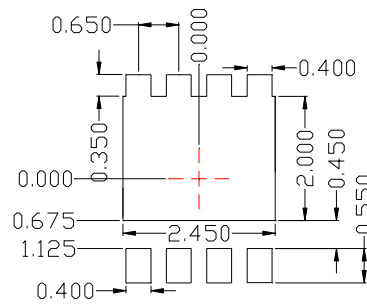


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

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