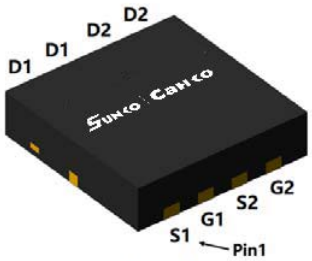
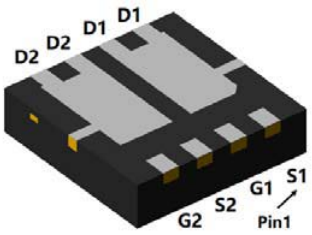
# N-Channel Enhancement Mode Field Effect Transistor

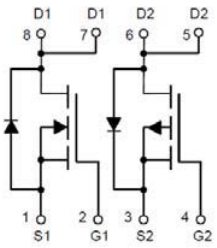



Top View




Bottom View

DFN3333-8L




## Product Summary

- $V_{DS}$ 30V
- $I_D$ 30A
- $R_{DS(ON)}$( at $V_{GS}$= 10V) ＜13mohm
- $R_{DS(ON)}$( at $V_{GS}$= 4.5V) ＜16mohm
- 100% EAS Tested

## General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- High current load applications
- Load switch
- Hard switched and high frequency circuits
- Uninterruptible power supply

## ■ Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | 30 | V |
| Gate-source Voltage | | $V_{GS}$ | ±20 | V |
| Drain Current | $T_A$=25℃ | $I_D$ | 9.7 | A |
| | $T_A$=100℃ | | 6.1 | |
| | $T_C$=25℃ | | 30 | |
| | $T_C$=100℃ | | 21 | |
| Pulsed Drain Current [A] | | $I_{DM}$ | 115 | A |
| Total Power Dissipation[B] | $T_A$=25℃ | $P_D$ | 2 | W |
| | $T_A$=100℃ | | 0.8 | |
| | $T_C$=25℃ | | 21 | |
| | $T_C$=100℃ | | 10.5 | |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 140 | mJ |
| Thermal Resistance-Junction to Ambient [C] | | $R_{\theta JA}$ | 60 | ℃/ W |
| Thermal Resistance Junction-to-Case | | $R_{\theta JC}$ | 7.1 | ℃/ W |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | ℃ |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| SCQ3622A | F1 | Q3622 | 5000 | 10000 | 100000 | 13“ reel |

## ■ Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=250μA | | 30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=30V,$V_{GS}$=0V | $T_J$=25℃ | | | 1 | μA |
| | | | $T_J$=55℃ | | | 5 | |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±20V, $V_{DS}$=0V | | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=250μA | | 1.0 | 1.5 | 2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$= 10V, $I_D$=20A | | | 7.5 | 13 | mΩ |
| | | $V_{GS}$= 4.5V, $I_D$=10A | | | 11.5 | 16 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=15A,$V_{GS}$=0V | | | 0.85 | 1.2 | V |
| Maximum Body-Diode Continuous Current | $I_S$ | | | | | 30 | A |
| **Dynamic Parameters** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=15V,$V_{GS}$=0V,f=1MHZ | | | 1015 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 201 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 164 | | |
| **Switching Parameters** | | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=10V,$V_{DS}$=20V,$I_D$=20A | | | 23.6 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | | 3.9 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | | 7.0 | | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=15A, di/dt=100A/us | | | 0.2 | | |
| Reverse Recovery Time | $t_{rr}$ | | | | 5 | | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=10V,$V_{DD}$=20V, $I_D$=2A, $R_{GEN}$=3Ω | | | 7 | | |
| Turn-on Rise Time | $t_r$ | | | | 19 | | |
| Turn-off Delay Time | $t_{D(off)}$ | | | | 24 | | |
| Turn-off fall Time | $t_f$ | | | | 24 | | |

A. Repetitive rating; pulse width limited by max. junction temperature.
B. $P_d$ is based on max. junction temperature, using junction-case thermal resistance.
C. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in the still air environment with $T_A$ =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

## ■ Typical Performance Characteristics

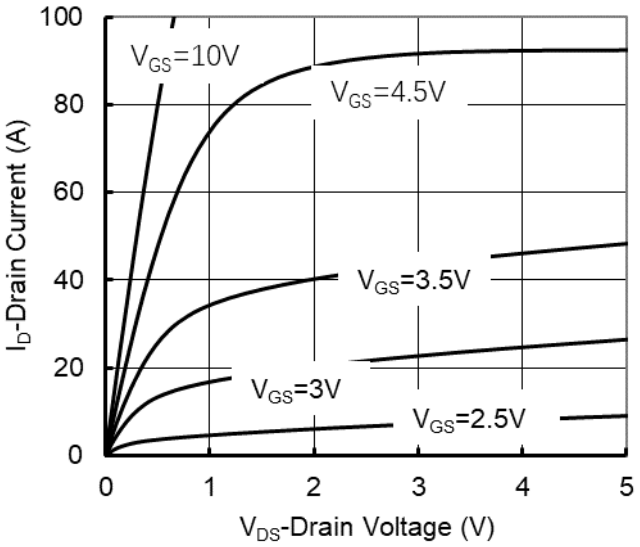



**Figure1. Output Characteristics**

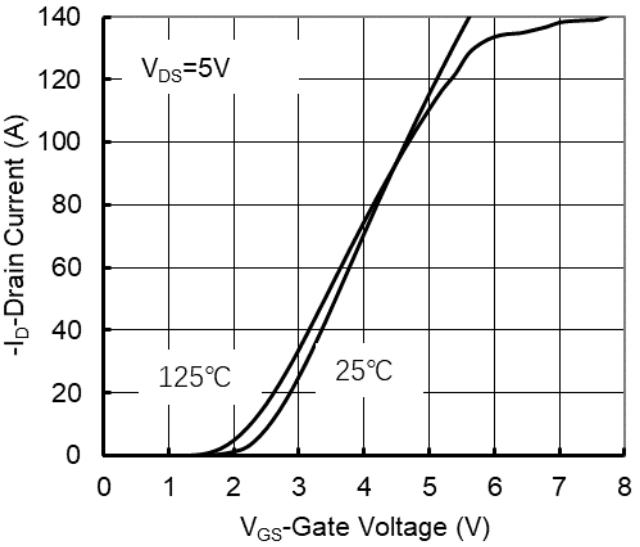



**Figure2. Transfer Characteristics**

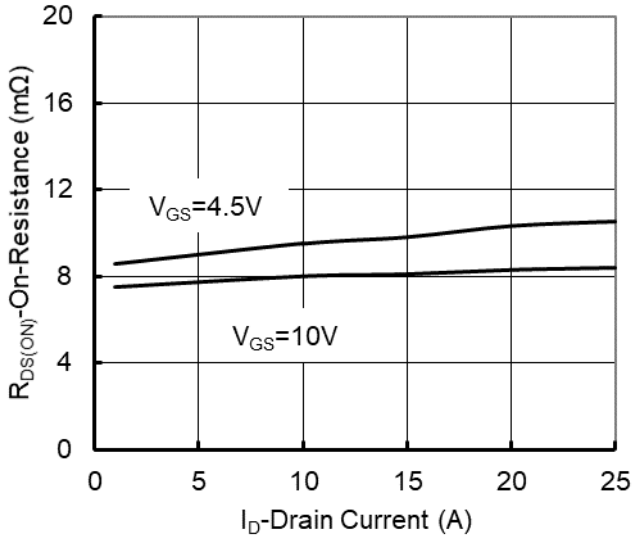



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

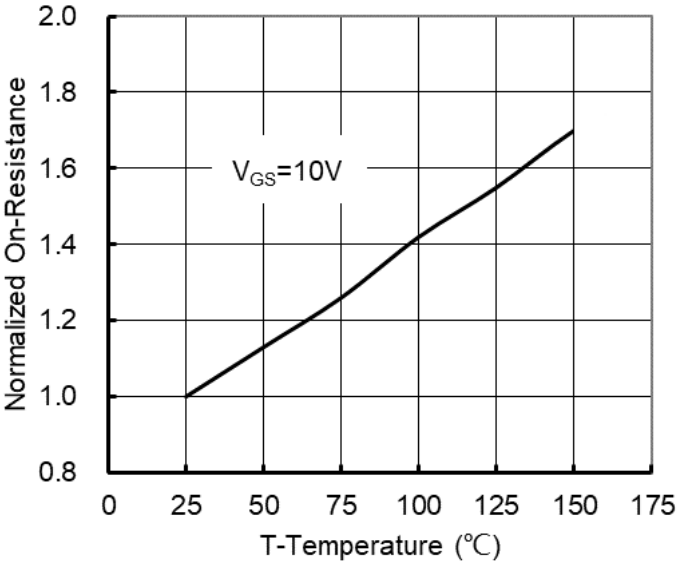



**Figure 4: On-Resistance vs. Junction Temperature**

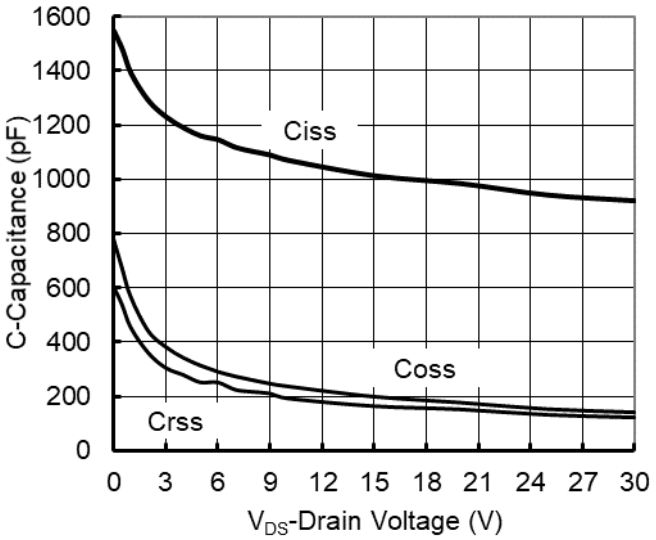



**Figure5. Capacitance Characteristics**

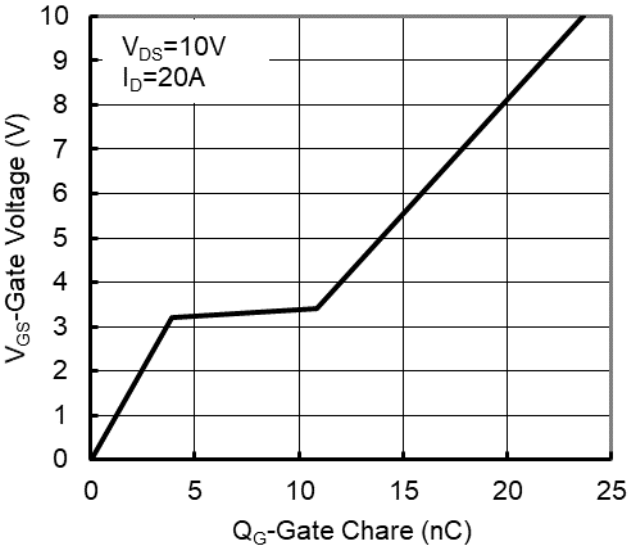



**Figure6. Gate Charge**

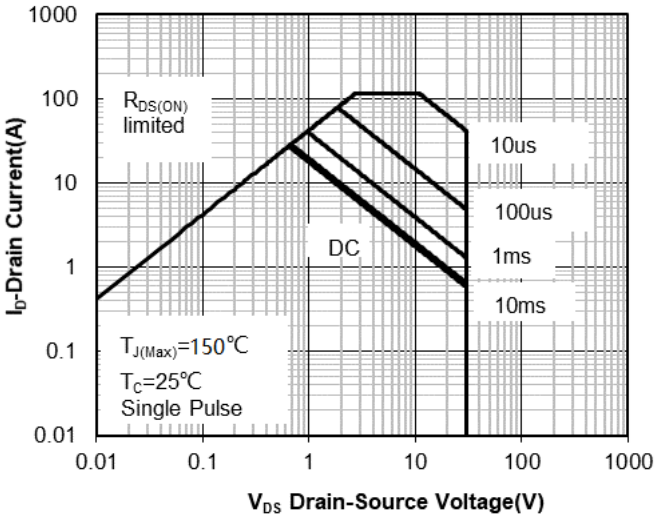



Figure7. Safe Operation Area

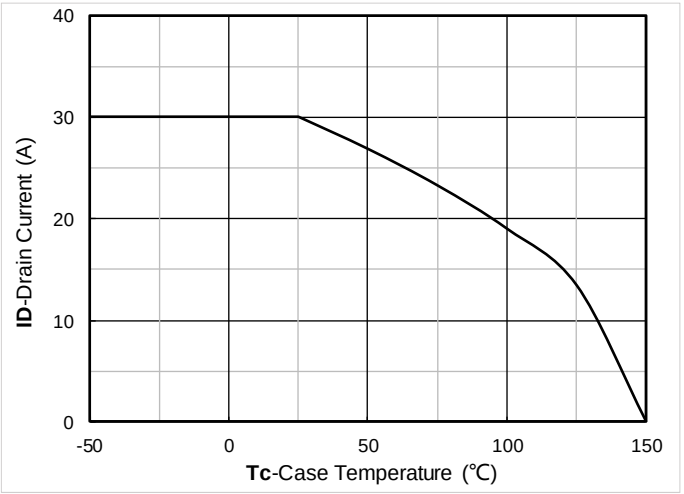



Figure8. Maximum Continuous Drain Current vs Case Temperature

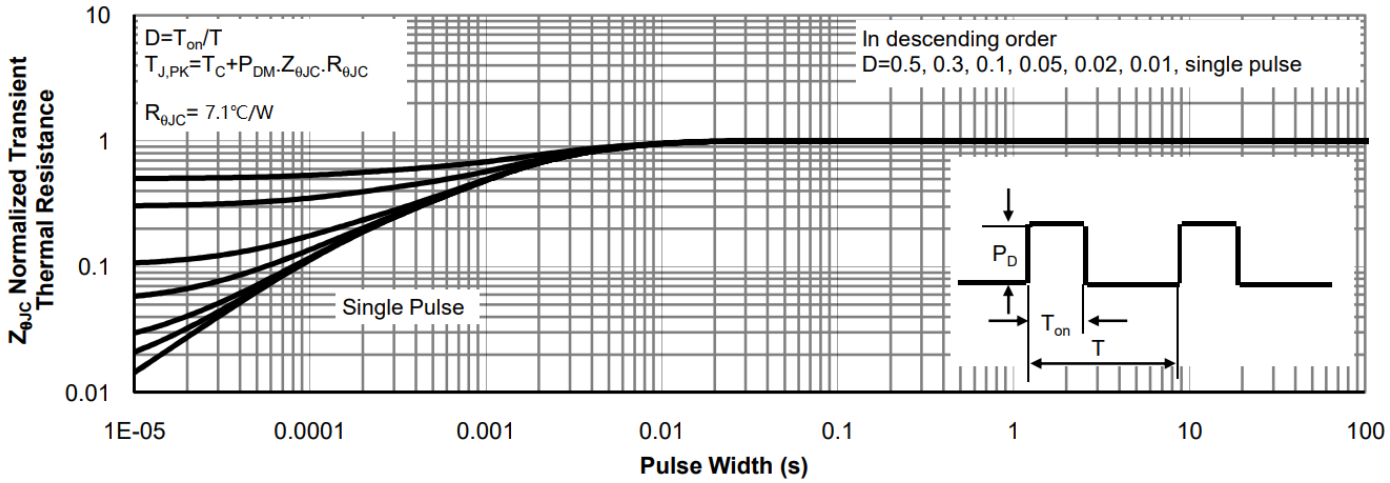
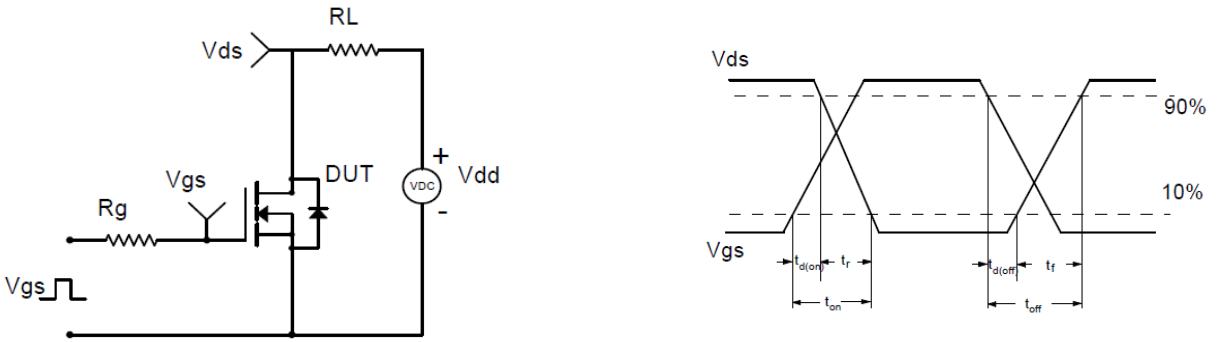
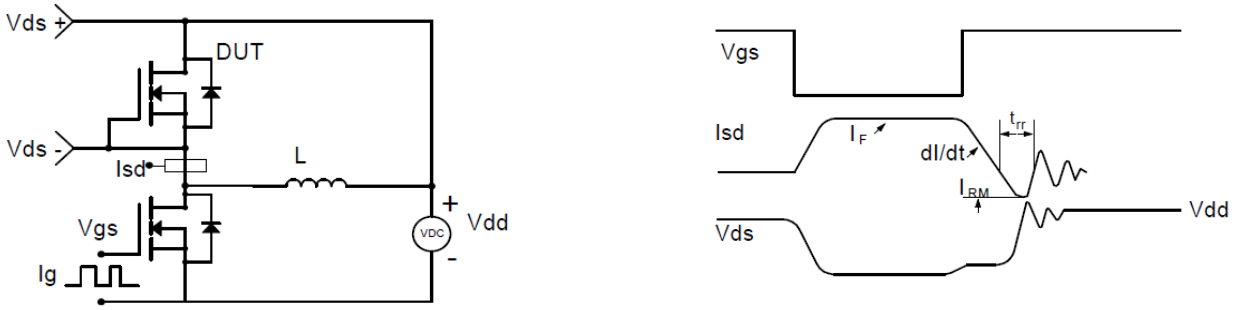


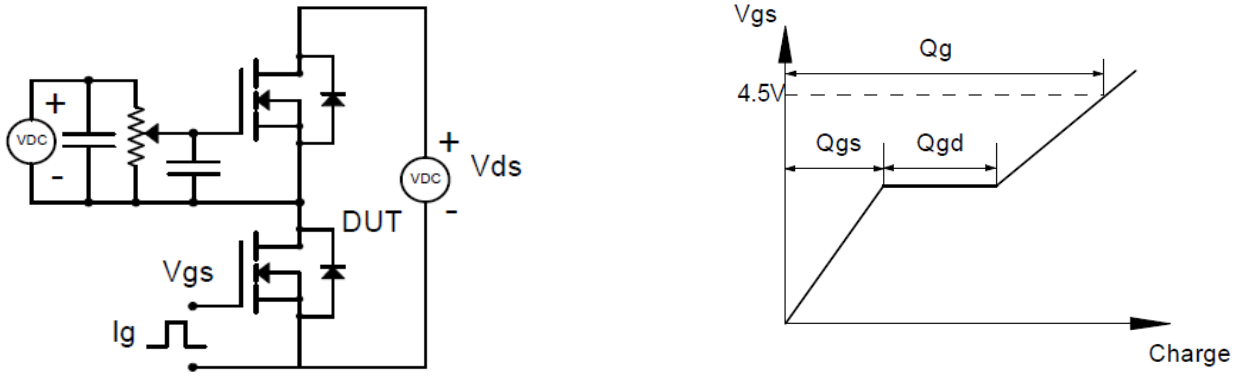

Figure9.Normalized Maximum Transient Thermal Impedance



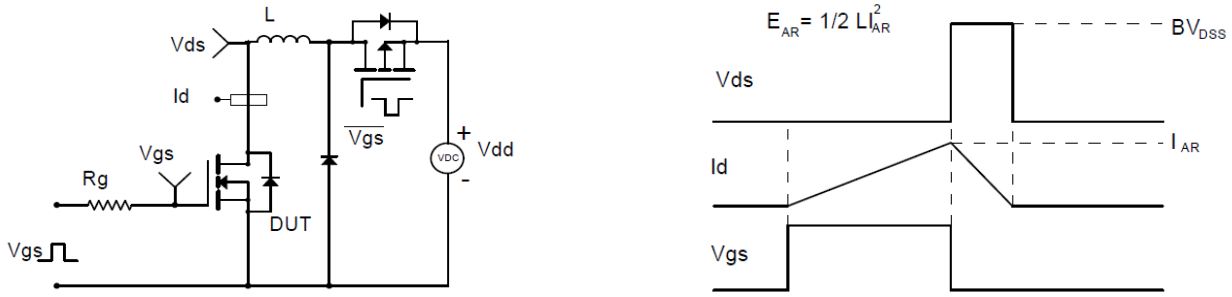

**Resistive Switching Test Circuit & Waveforms**




**Diode Recovery Test Circuit & Waveforms**

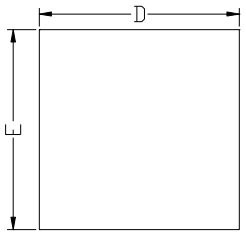



**Gate Charge Test Circuit & Waveform**

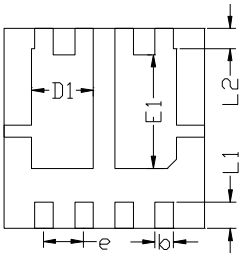



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

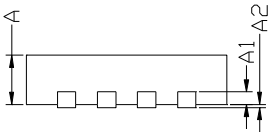
## ■DFN3333-8L Package information




Top View
正面视图



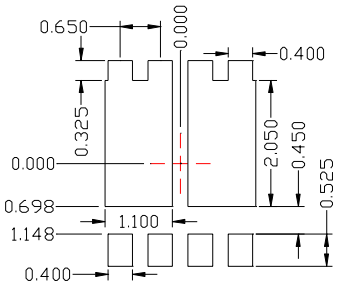

Bottom View
背面视图




Side View
侧面视图

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 3.15 | 3.25 | 3.35 |
| E | 3.15 | 3.25 | 3.35 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | | 0.20 BSC | |
| A2 | | | 0.10 |
| D1 | 0.90 | 1.00 | 1.10 |
| E1 | 1.75 | 1.85 | 1.95 |
| L1 | 0.325 | 0.425 | 0.525 |
| L2 | | 0.325 BSC | |
| b | 0.20 | 0.30 | 0.40 |
| e | | 0.65 BSC | |

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.




Suggested Solder Pad Layout
Top View

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