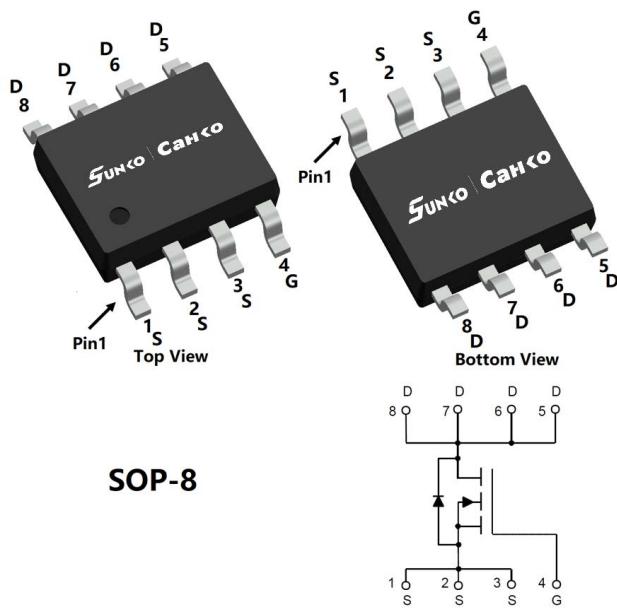


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- V<sub>DS</sub> 60V
- I<sub>D</sub> 12A
- R<sub>DS(ON)</sub>( at V<sub>GS</sub>=10V) <8.5 mohm
- R<sub>DS(ON)</sub>( at V<sub>GS</sub>=4.5V) <12 mohm
- 100% EAS Tested

### General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low R<sub>DS(ON)</sub>
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

#### Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V <sub>DS</sub>	60	V
Gate-source Voltage	V <sub>GS</sub>	±20	V
Drain Current (Silicon limited)	I <sub>D</sub>	12	A
T <sub>A</sub> =100°C		7.5	
Pulsed Drain Current <sup>A</sup>	I <sub>DM</sub>	48	A
Avalanche energy <sup>B</sup>	E <sub>AS</sub>	132	mJ
Total Power Dissipation <sup>C</sup>	P <sub>D</sub>	3.1	W
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55~+150	°C

#### Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	R <sub>θJA</sub>	31	40	°C/W
Thermal Resistance Junction-to-Ambient <sup>D</sup>		59	75	
Thermal Resistance Junction-to-Case	R <sub>θJL</sub>	16	24	

#### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCS12G06D	F2	Q12G06D	4000	8000	64000	13" reel

■ Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$	$T_J=25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J=55^\circ\text{C}$		5	
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			$\pm 100$	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=12\text{A}$		6.8	8.5	$\text{m}\Omega$
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=10\text{A}$		8.3	12	
Diode Forward Voltage	$V_{\text{SD}}$	$I_{\text{S}}=12\text{A}, V_{\text{GS}}=0\text{V}$		0.85	1.3	V
Maximum Body-Diode Continuous Current	$I_{\text{S}}$				12	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=35\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		2000		$\text{pF}$
Output Capacitance	$C_{\text{oss}}$			390		
Reverse Transfer Capacitance	$C_{\text{rss}}$			13		
Gate Resistance	$R_g$	$f=1\text{MHz}, \text{Open drain}$		1.6		$\Omega$
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DS}}=30\text{V}, I_{\text{D}}=12\text{A}$		34		$\text{nC}$
Total Gate Charge	$Q_g(4.5\text{V})$			15.8		
Gate-Source Charge	$Q_{\text{gs}}$			7.8		
Gate-Drain Charge	$Q_{\text{gd}}$			5.2		
Reverse Recovery Charge	$Q_{\text{rr}}$	$I_F=12\text{A}, dI/dt=200\text{A/us}$		36		$\text{ns}$
Reverse Recovery Time	$t_{\text{rr}}$			27		
Turn-on Delay Time	$t_{\text{D(on)}}$			10		
Turn-on Rise Time	$t_r$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=30\text{V}, I_{\text{D}}=12\text{A}$ $R_{\text{GEN}}=3\Omega$		36		$\text{ns}$
Turn-off Delay Time	$t_{\text{D(off)}}$			30		
Turn-off fall Time	$t_f$			57		

A. Repetitive rating; pulse width limited by max. junction temperature.

B.  $V_{\text{DD}}=50\text{V}, R_G=25\Omega, L=0.5\text{mH}, I_{\text{AS}}=23\text{A}.$ C.  $P_d$  is based on max. junction temperature, using  $\leq 10\text{s}$  junction-ambient thermal resistance.D. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $TA = 25^\circ\text{C}$ . The Power dissipation PDSM is based on  $R_{\theta JA} \leq 10\text{s}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

## ■ Typical Performance Characteristics

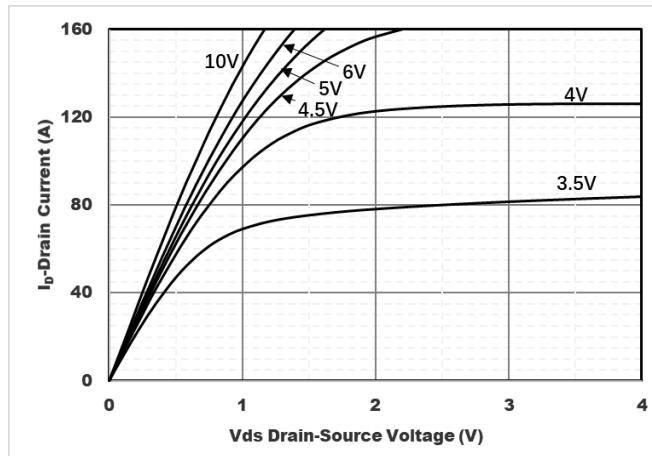


Figure1. Output Characteristics

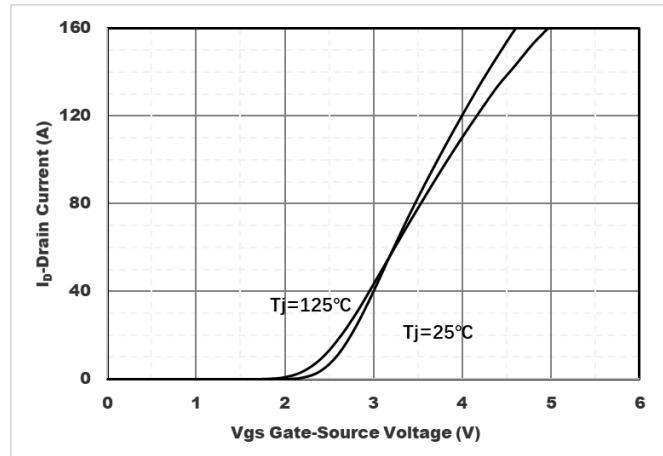


Figure2. Transfer Characteristics

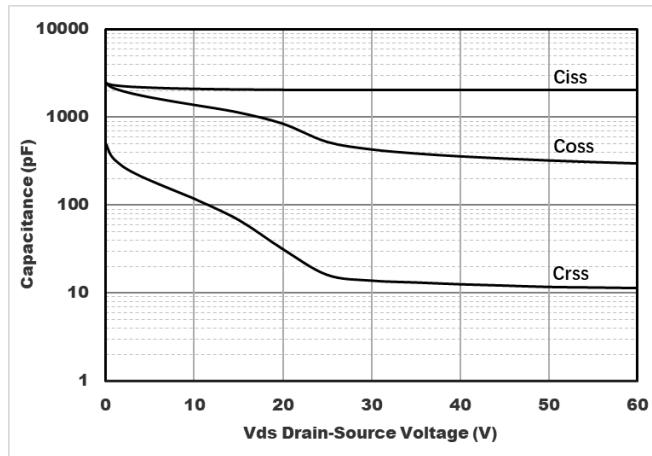


Figure3. Capacitance Characteristics

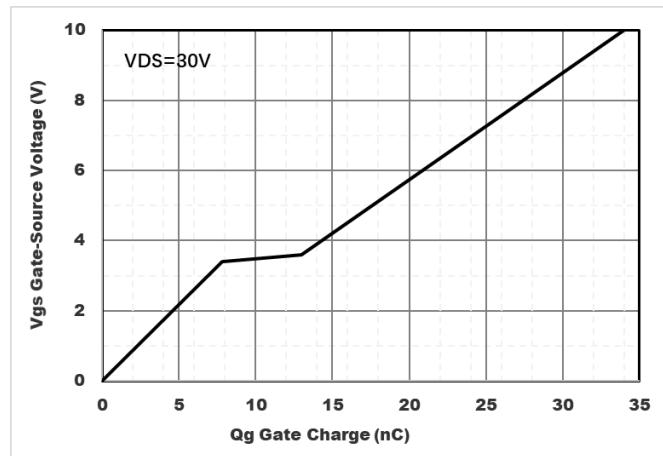


Figure4. Gate Charge

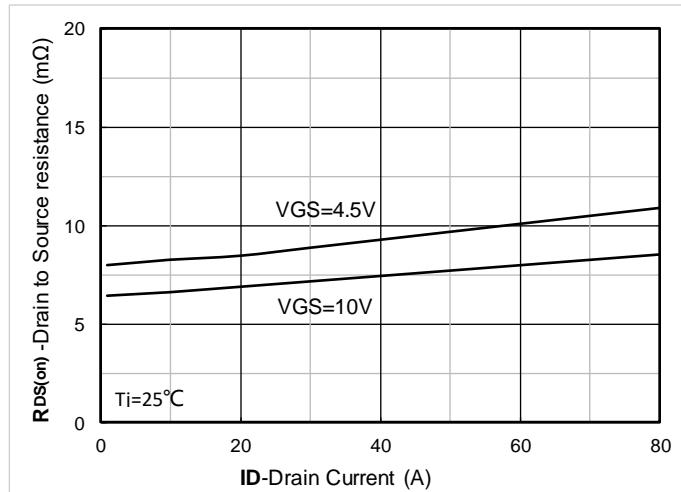


Figure5. Drain-Source on Resistance

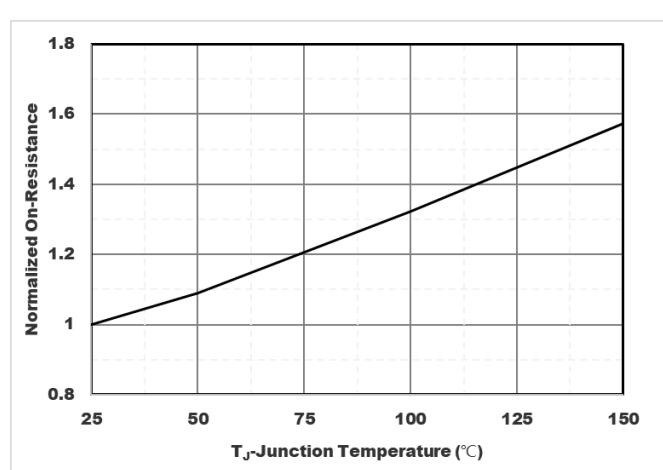


Figure6. Normalized On-Resistance

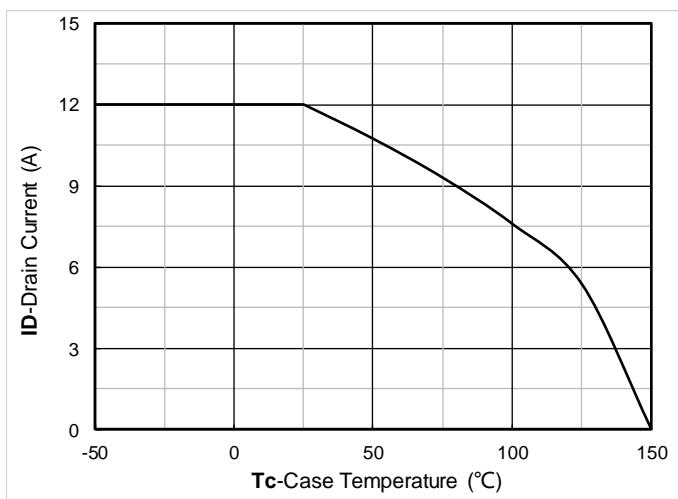


Figure 7. Drain current

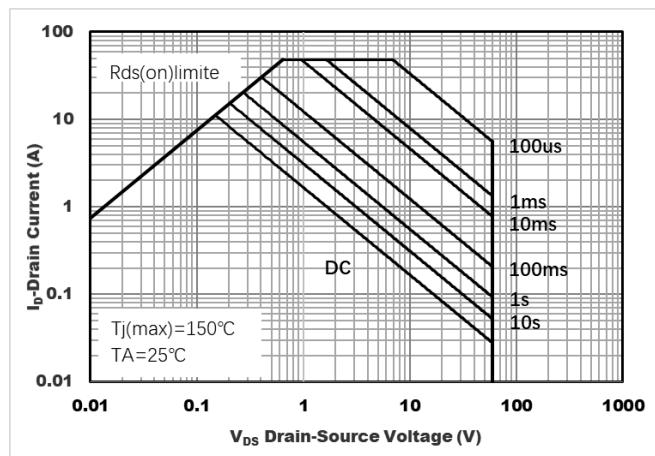


Figure 8. Safe Operation Area

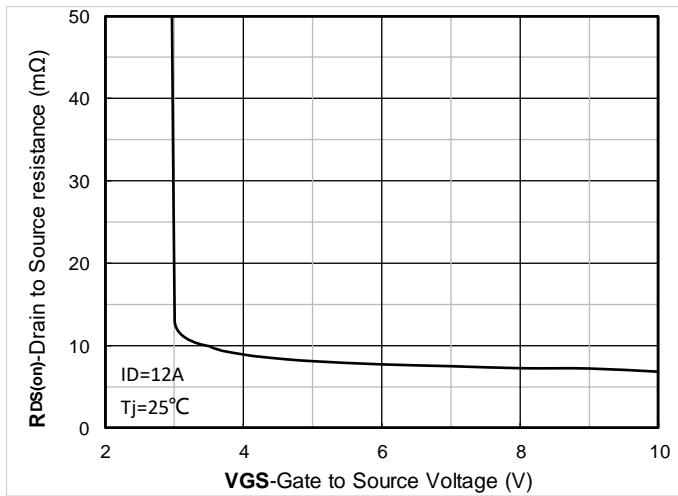


Figure 9. On-Resistance vs Gate to Source Voltage

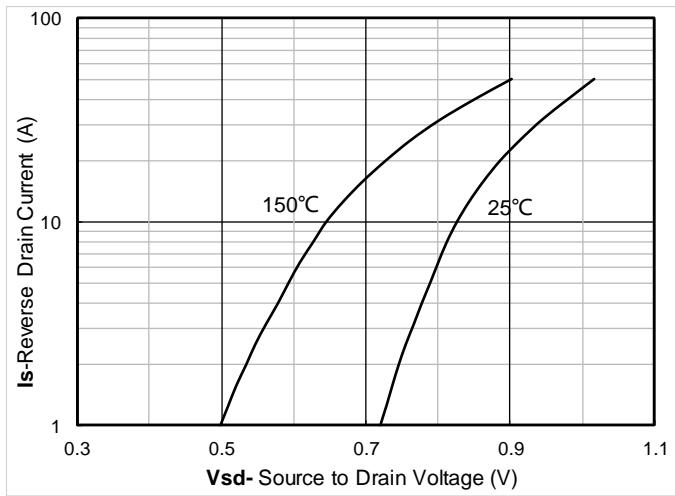


Figure 10. Forward characteristics of reverse diode

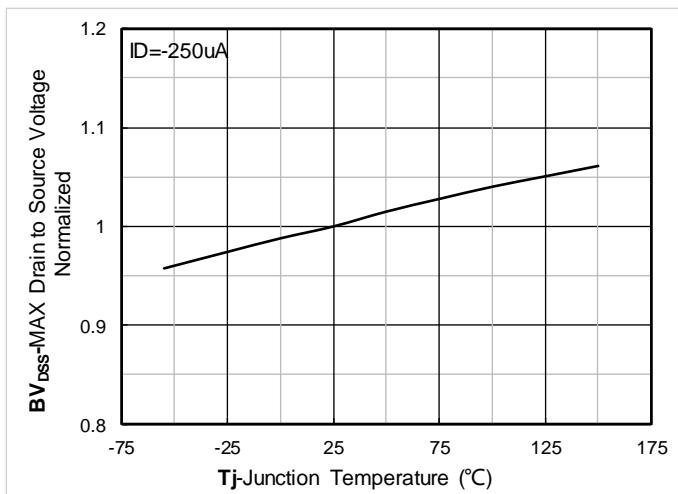


Figure 11. Normalized breakdown voltage

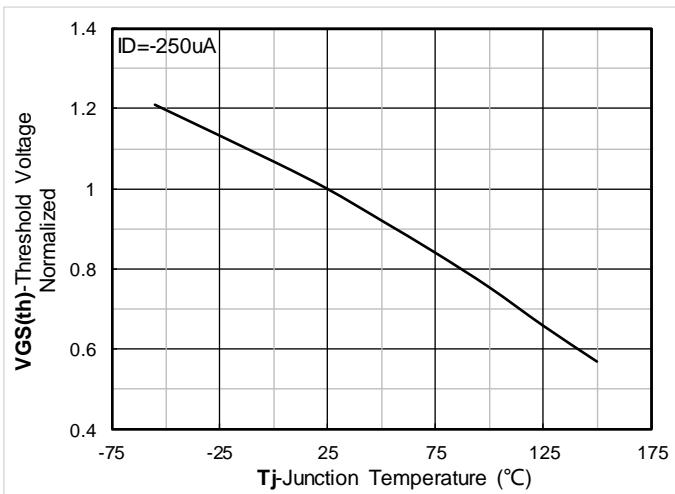


Figure 12. Normalized Threshold voltage

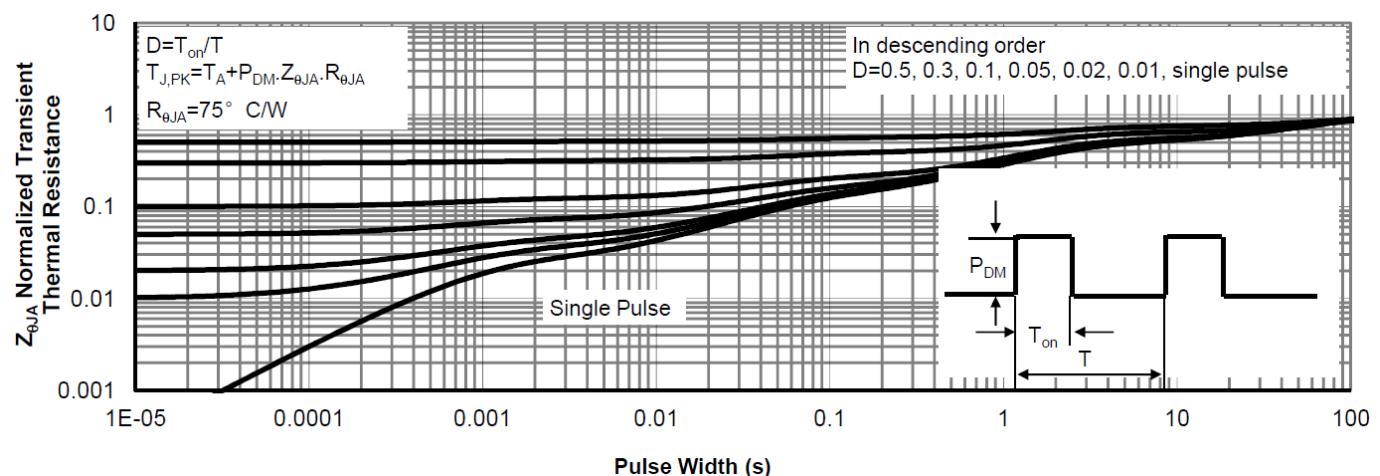
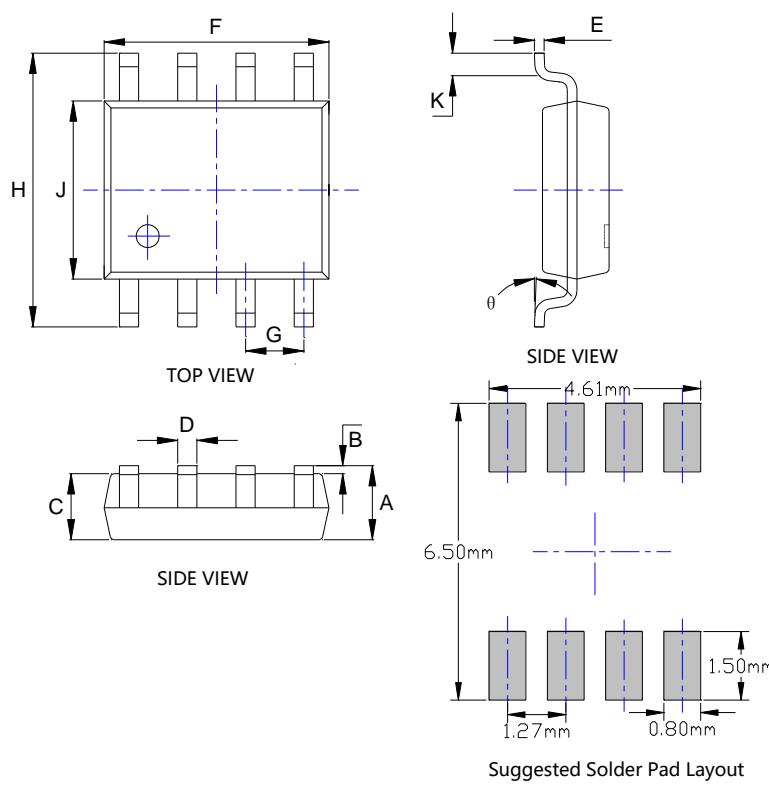


Figure13. Normalized Maximum Transient Thermal Impedance

## ■ SOP-8 Package information



SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
theta	0°	8°	0°	8°

### Note:

1. Controlling dimension: in millimeters.
2. General tolerance: +/-0.05mm.
3. The pad layout is for reference purposes only.

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