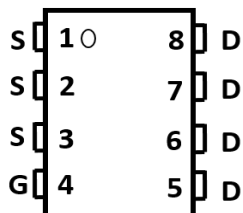
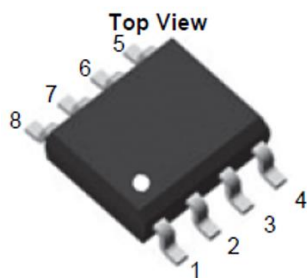
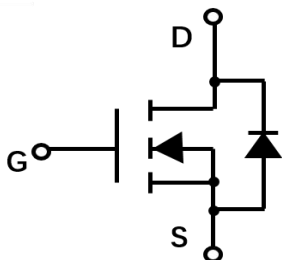


## N-Channel Enhancement Mode Field Effect Transistor



**SOP-8**



### Product Summary

- $V_{DS}$  60V
- $I_D$  8.2A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <22mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <34mohm

### General Description

- Trench Power MV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| Parameter                              |                       | Symbol                            | Limit    | Unit  |
|----------------------------------------|-----------------------|-----------------------------------|----------|-------|
| Drain-source Voltage                   |                       | V <sub>DS</sub>                   | 60       | V     |
| Gate-source Voltage                    |                       | V <sub>GS</sub>                   | ± 20     | V     |
| Drain Current <sup>A</sup>             | T <sub>A</sub> =25 °C | I <sub>D</sub>                    | 8.2      | A     |
|                                        | T <sub>A</sub> =70 °C |                                   | 6.6      |       |
| Pulsed Drain Current <sup>B</sup>      |                       | I <sub>DM</sub>                   | 39       | A     |
| Total Power Dissipation                | T <sub>A</sub> =25 °C | P <sub>D</sub>                    | 3.1      | W     |
|                                        | T <sub>A</sub> =70 °C |                                   | 2        |       |
| Thermal Resistance Junction-to-Ambient | t≤ 10s                | R <sub>θJA</sub>                  | 40       | °C/ W |
|                                        | Steady-State          |                                   | 75       |       |
| Thermal Resistance Junction-to-Case    | Steady-State          | R <sub>θJL</sub>                  | 30       | °C/ W |
| Junction and Storage Temperature Range |                       | T <sub>J</sub> , T <sub>STG</sub> | -55~+150 | °C    |

### ■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| SCS4438A      | F2           | Q4438   | 4000                 | 8000                    | 64000                      | 13" reel      |

## ■ Electrical Characteristics (T<sub>J</sub>=25℃ unless otherwise noted)

| Parameter                             | Symbol              | Conditions                                                                          | Min | Typ  | Max  | Units |
|---------------------------------------|---------------------|-------------------------------------------------------------------------------------|-----|------|------|-------|
| Static Parameter                      |                     |                                                                                     |     |      |      |       |
| Drain-Source Breakdown Voltage        | BV <sub>DSS</sub>   | V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA                                         | 60  |      |      | V     |
| Zero Gate Voltage Drain Current       | I <sub>DSS</sub>    | V <sub>DS</sub> =60V,V <sub>GS</sub> =0V                                            |     |      | 1    | μA    |
| Gate-Body Leakage Current             | I <sub>GSS</sub>    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V                                         |     |      | ±100 | nA    |
| Gate Threshold Voltage                | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA                           | 1.0 | 1.5  | 2.5  | V     |
| Static Drain-Source On-Resistance     | R <sub>DS(ON)</sub> | V <sub>GS</sub> = 10V, I <sub>D</sub> =8.2A                                         |     | 14.5 | 22   | mΩ    |
|                                       |                     | V <sub>GS</sub> = 4.5V, I <sub>D</sub> =7.6A                                        |     | 17   | 34   |       |
| Diode Forward Voltage                 | V <sub>SD</sub>     | I <sub>S</sub> =8.2A, V <sub>GS</sub> =0V                                           |     | 0.8  | 1.2  | V     |
| Maximum Body-Diode Continuous Current | I <sub>S</sub>      |                                                                                     |     |      | 8.2  | A     |
| Dynamic Parameters                    |                     |                                                                                     |     |      |      |       |
| Input Capacitance                     | C <sub>iss</sub>    | V <sub>DS</sub> =30V,V <sub>GS</sub> =0V,f=1MHZ                                     |     | 2027 |      | pF    |
| Output Capacitance                    | C <sub>oss</sub>    |                                                                                     |     | 132  |      |       |
| Reverse Transfer Capacitance          | C <sub>rss</sub>    |                                                                                     |     | 116  |      |       |
| Switching Parameters                  |                     |                                                                                     |     |      |      |       |
| Total Gate Charge                     | Q <sub>g</sub>      | V <sub>GS</sub> =10V,V <sub>DS</sub> =30V,I <sub>D</sub> =10A                       |     | 51   |      | nC    |
| Gate-Source Charge                    | Q <sub>gs</sub>     |                                                                                     |     | 8.1  |      |       |
| Gate-Drain Charge                     | Q <sub>gd</sub>     |                                                                                     |     | 11.4 |      |       |
| Reverse Recovery Chrage               | Q <sub>rr</sub>     | I <sub>F</sub> =20A, di/dt=500A/us                                                  |     | 11.4 |      | ns    |
| Reverse Recovery Time                 | t <sub>rr</sub>     |                                                                                     |     | 22   |      |       |
| Turn-on Delay Time                    | t <sub>D(on)</sub>  | V <sub>GS</sub> =10V,V <sub>DD</sub> =30V, I <sub>D</sub> =2A, R <sub>GEN</sub> =3Ω |     | 11   |      |       |
| Turn-on Rise Time                     | t <sub>r</sub>      |                                                                                     |     | 21   |      |       |
| Turn-off Delay Time                   | t <sub>D(off)</sub> |                                                                                     |     | 40   |      |       |
| Turn-off fall Time                    | t <sub>f</sub>      |                                                                                     |     | 23   |      |       |

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. R<sub>θJA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJL</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

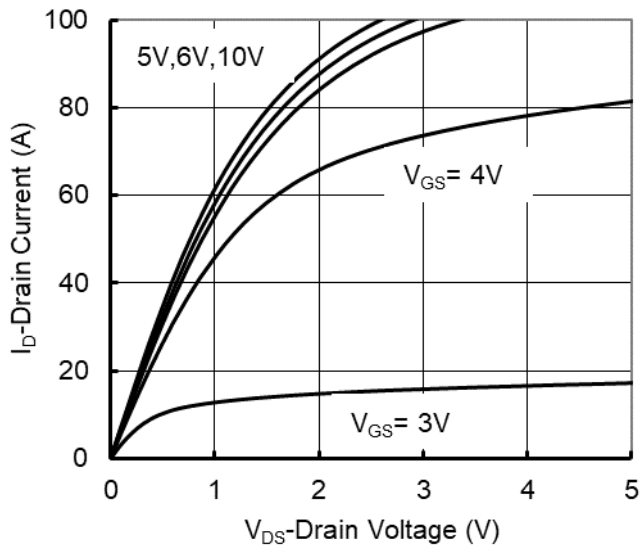


Figure 1. Output Characteristics

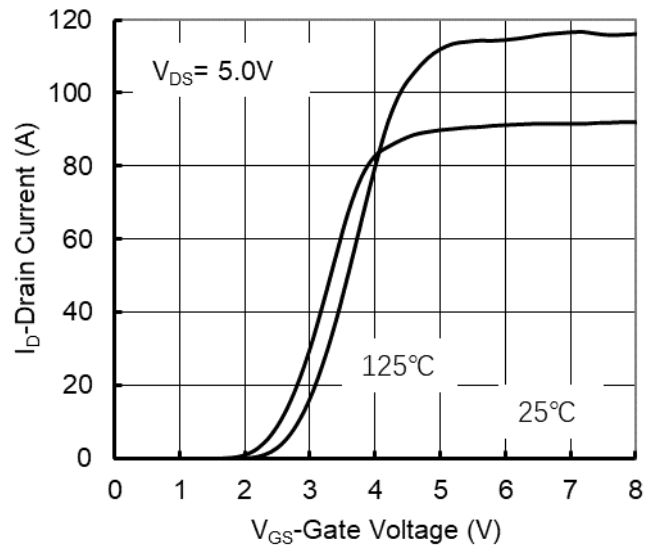


Figure 2. Transfer Characteristics

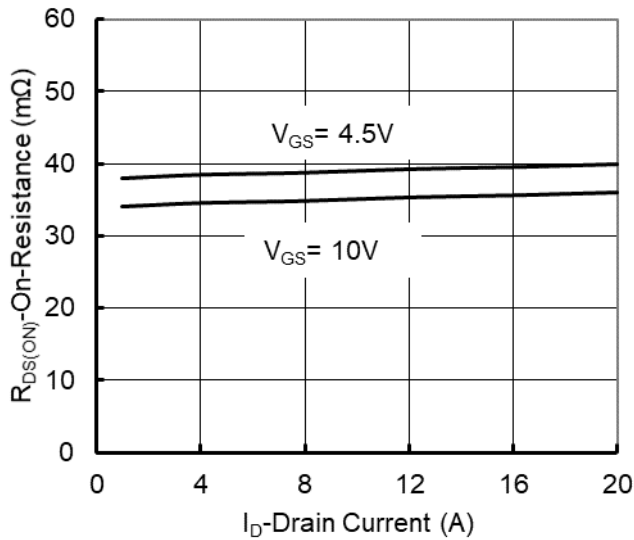


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

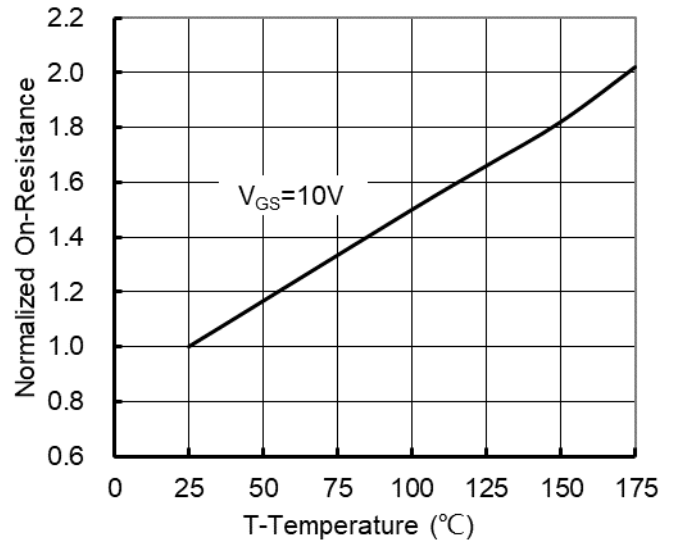


Figure 4. On-Resistance vs. Junction Temperature

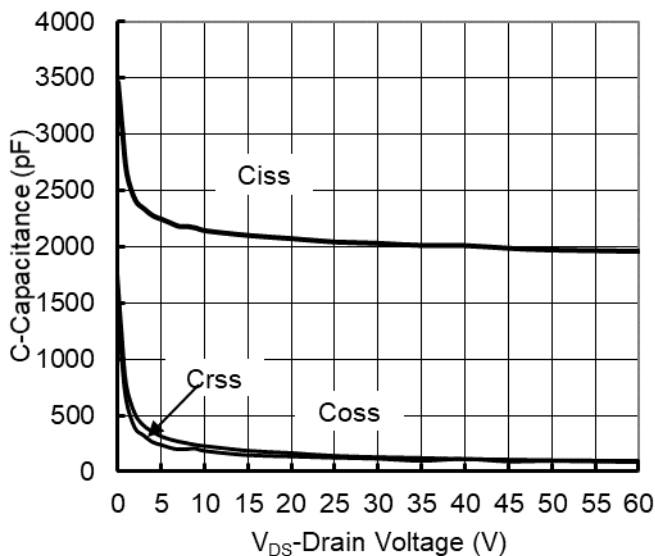


Figure 5. Capacitance Characteristics

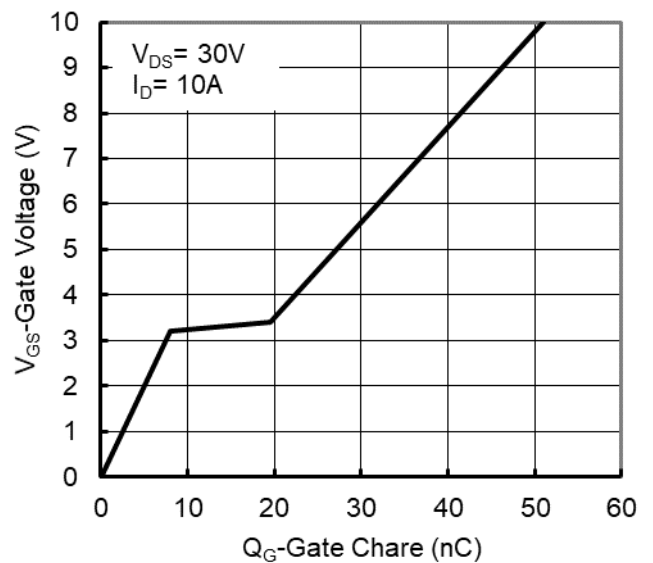


Figure 6. Gate Charge

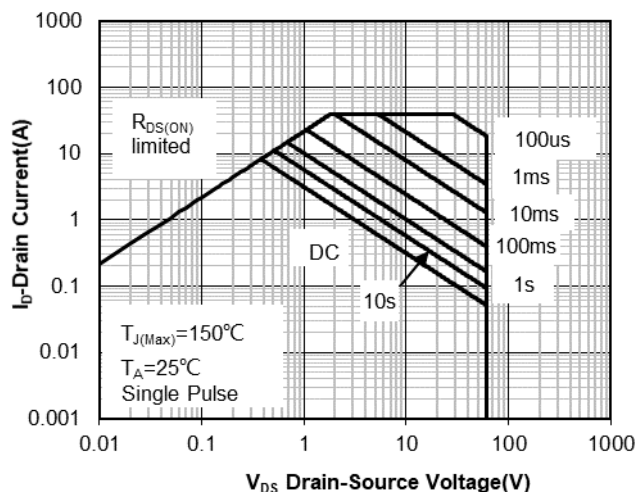


Figure 7. Safe Operation Area

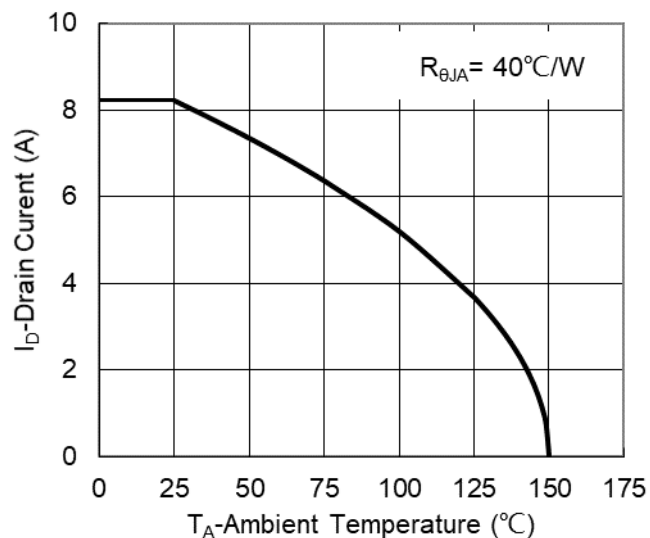


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

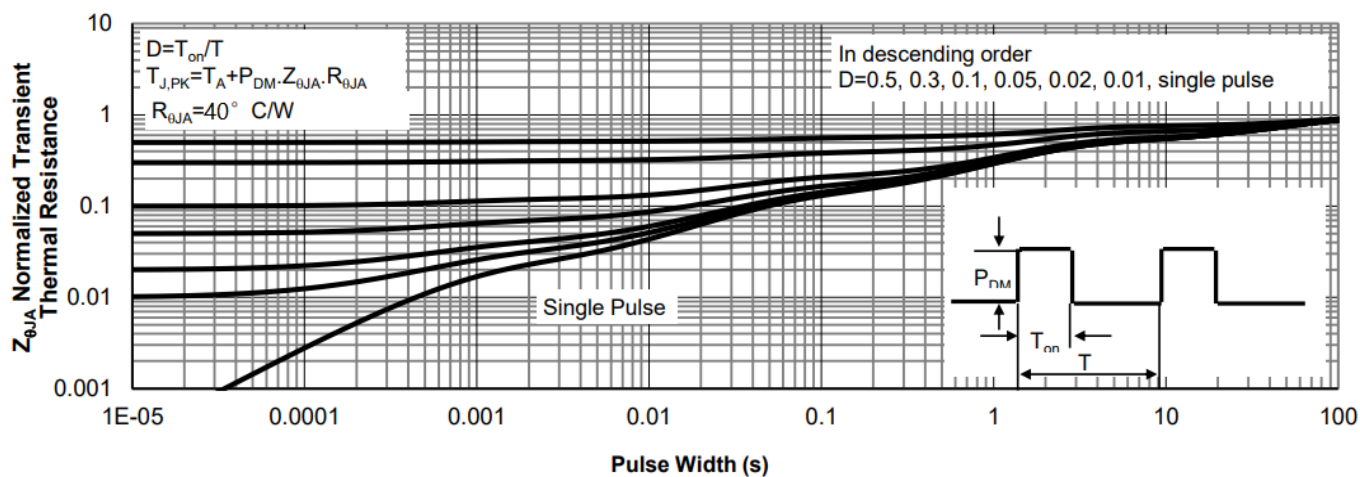
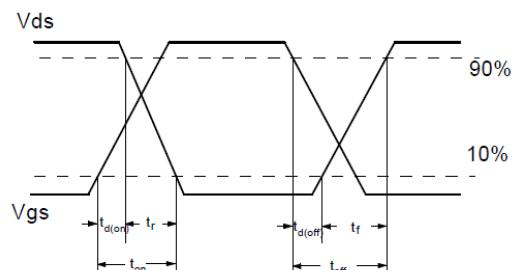
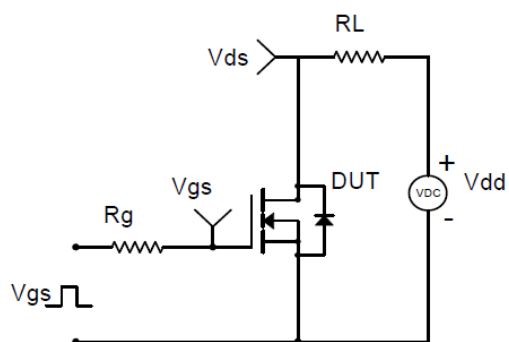
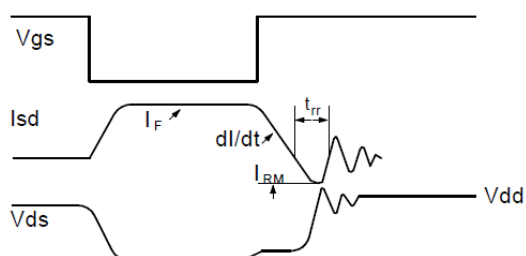
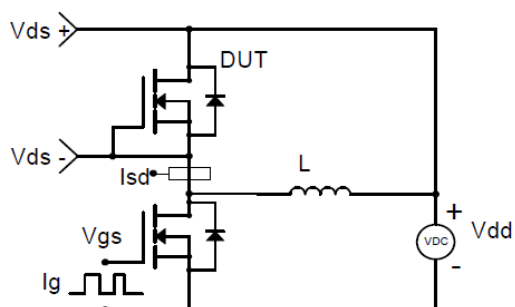


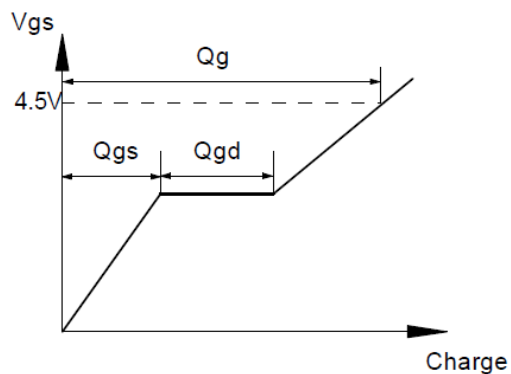
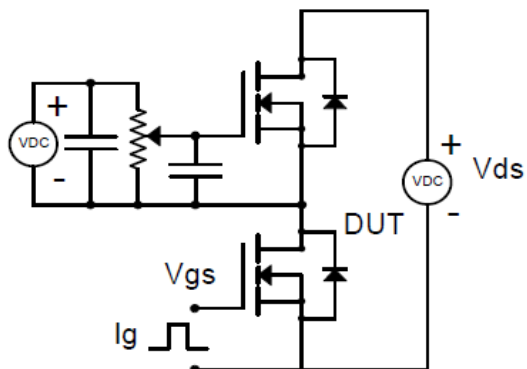
Figure 9. Normalized Maximum Transient Thermal Impedance



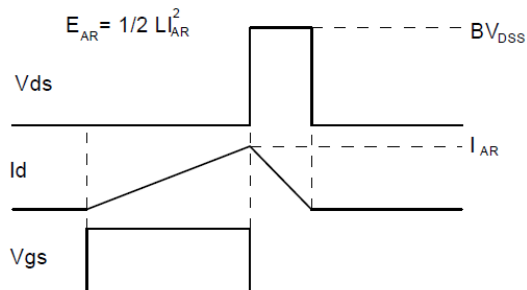
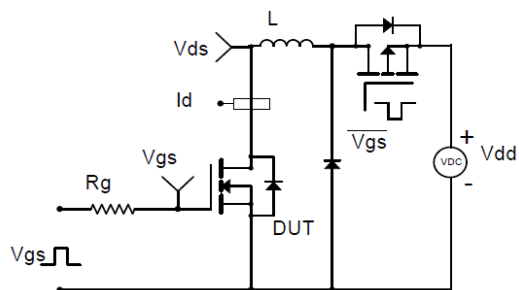
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

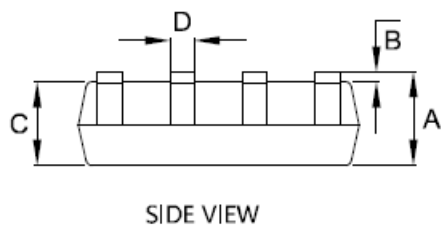
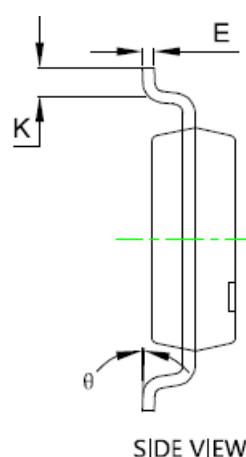
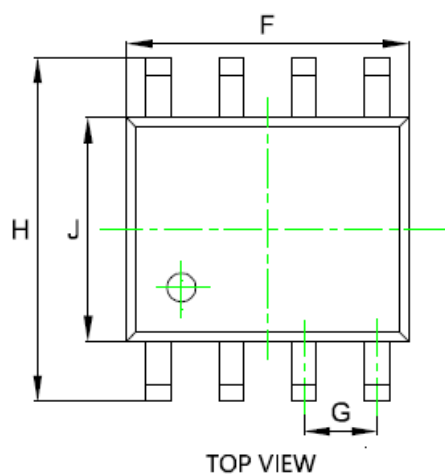


Gate Charge Test Circuit & Waveform

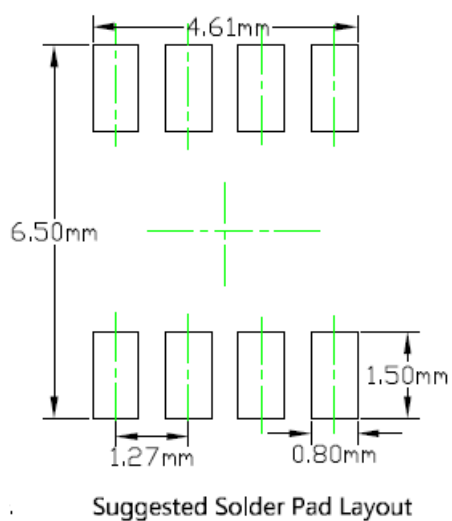


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■SOP-8 Package information



| SYMBOL | DIMENSIONS |       |            |       |
|--------|------------|-------|------------|-------|
|        | INCHES     |       | Millimeter |       |
|        | MIN.       | MAX.  | MIN.       | MAX.  |
| A      | 0.053      | 0.069 | 1.350      | 1.750 |
| B      | 0.004      | 0.010 | 0.100      | 0.250 |
| C      | 0.053      | 0.061 | 1.350      | 1.550 |
| D      | 0.013      | 0.020 | 0.330      | 0.510 |
| E      | 0.007      | 0.010 | 0.170      | 0.250 |
| F      | 0.189      | 0.197 | 4.800      | 5.000 |
| G      | 0.050BSC   |       | 1.270BSC   |       |
| H      | 0.228      | 0.244 | 5.800      | 6.200 |
| J      | 0.150      | 0.157 | 3.800      | 4.000 |
| K      | 0.016      | 0.050 | 0.400      | 1.270 |
| θ      | 0°         | 8°    | 0°         | 8°    |



Note:

1. Controlling dimension: in millimeters
2. General tolerance:  $\pm 0.5\text{mm}$ .
3. The pad layout is for reference purposes only.

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