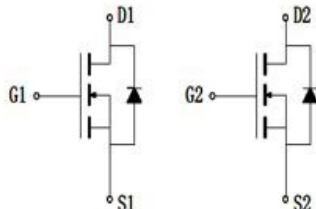
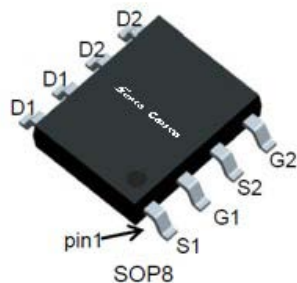


N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 30V
- I_D 12A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <12 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <15 mohm



General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

SOP-8

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$ @ Steady State	I_D	12	A
	$T_A=70^\circ\text{C}$ @ Steady State		9.6	
Pulsed Drain Current ^A		I_{DM}	50	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$		P_D	2.5	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCSD12N03A	F2	Q12N03..	4000	8000	64000	13" reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8.0A		7	12	mΩ
		V _{GS} = 4.5V, I _D =6.0A		11	15	
Diode Forward Voltage	V _{SD}	I _S =12A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				12	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		1015		pF
Output Capacitance	C _{oss}			201		
Reverse Transfer Capacitance	C _{rss}			164		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A		23.6		nC
Gate Source Charge	Q _{gs}			3.9		
Gate Drain Charge	Q _{gd}			7.0		
Reverse Recovery Chrage	Q _{rr}	I _F =15A, di/dt=100A/us		0.2		
Reverse Recovery Time	t _{rr}			5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _{GEN} =3Ω		7		ns
Turn-on Rise Time	t _r			20		
Turn-off Delay Time	t _{D(off)}			24		
Turn-off Fall Time	t _f			24		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. R_{θJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{θJL} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

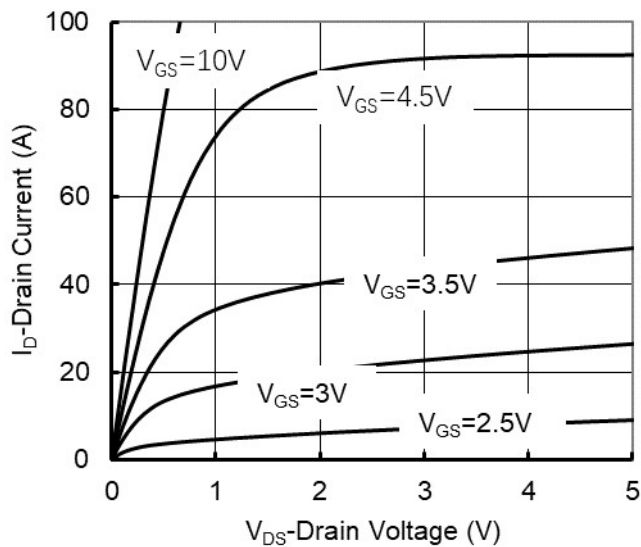


Figure1. Output Characteristics

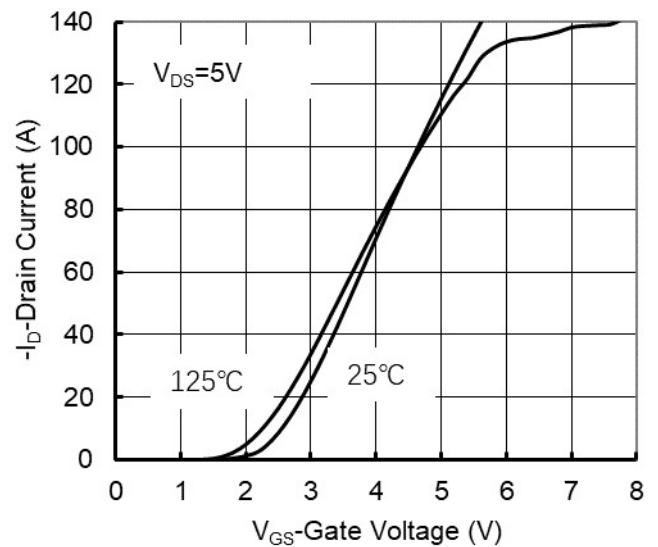


Figure2. Transfer Characteristics

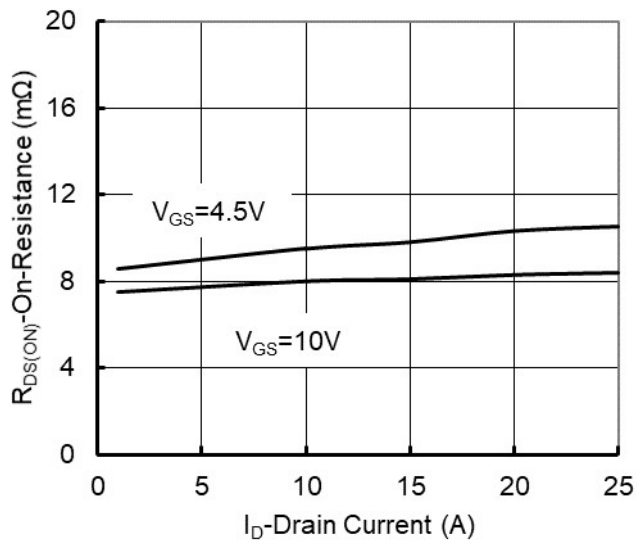


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

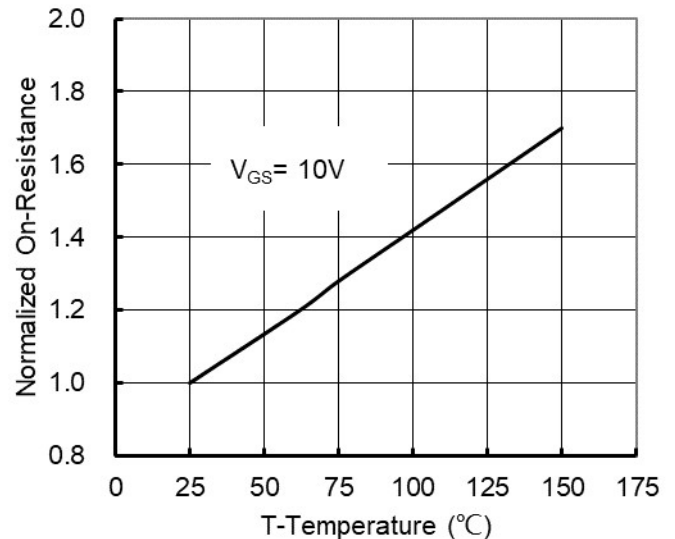


Figure 4: On-Resistance vs. Junction Temperature

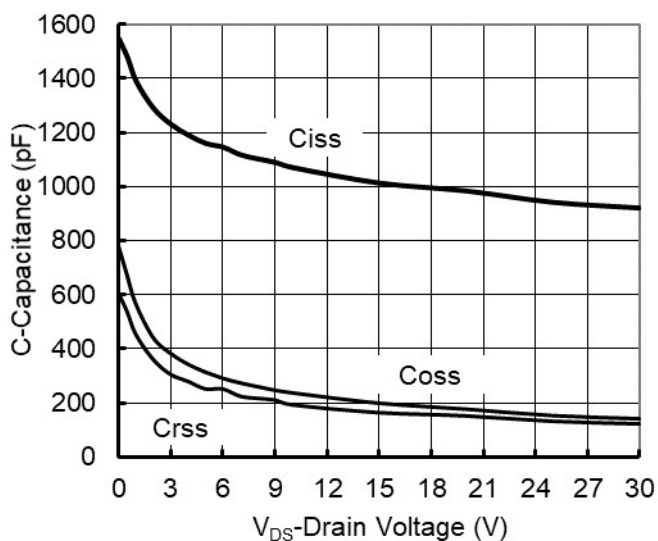


Figure5. Capacitance Characteristics

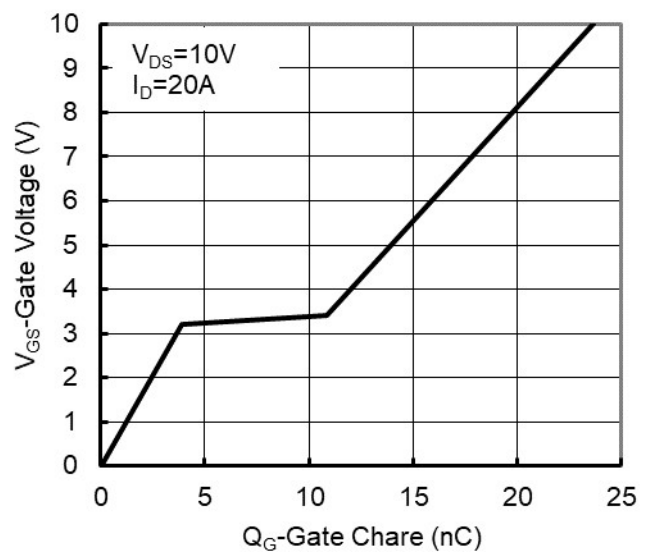


Figure6. Gate Charge

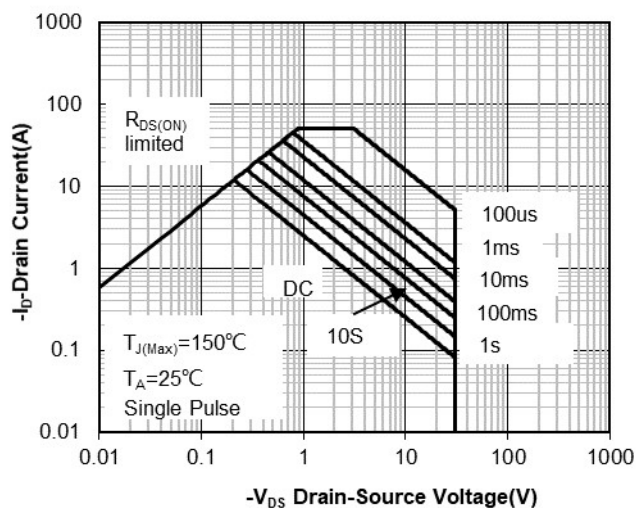


Figure7. Safe Operation Area

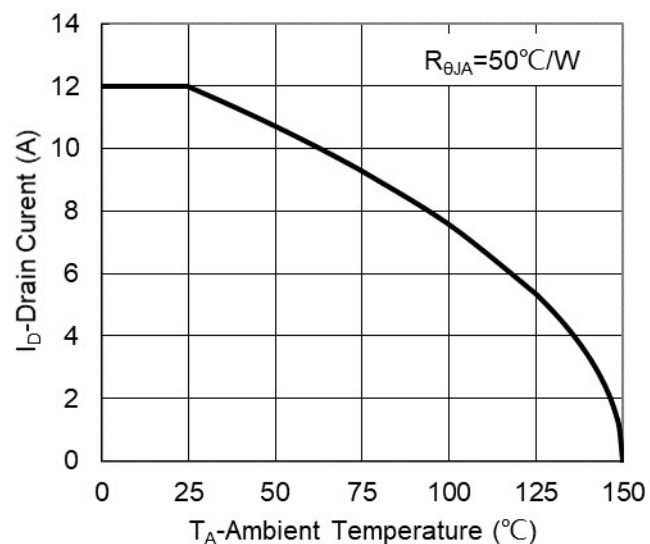


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

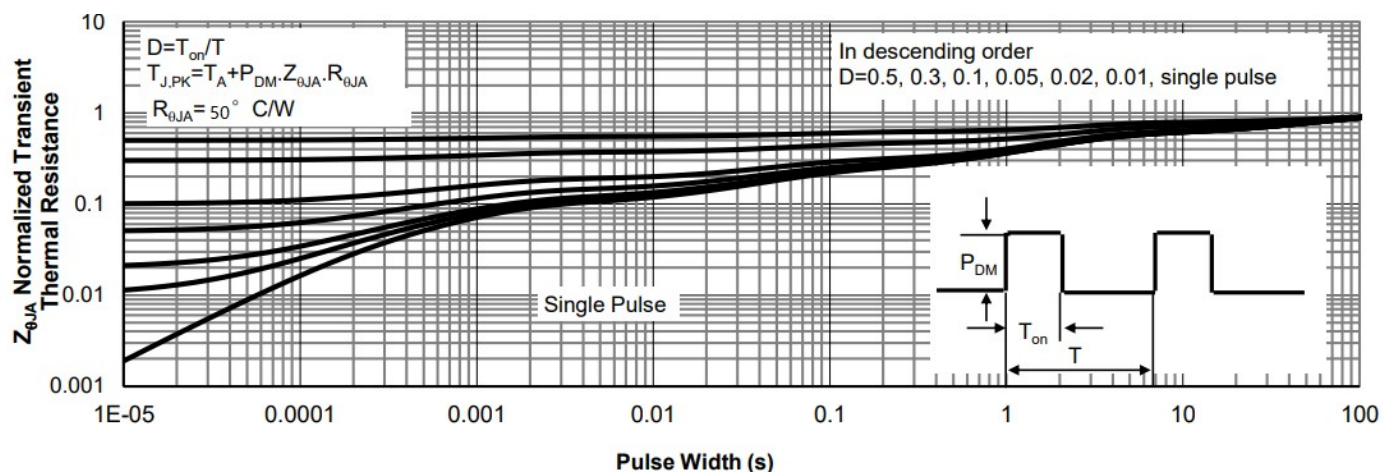
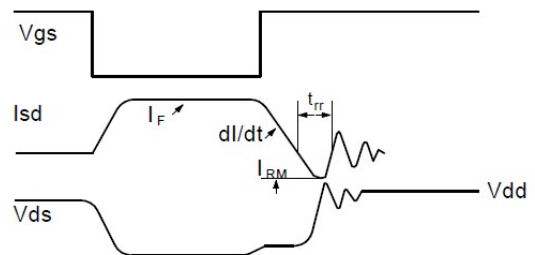


Figure9. Normalized Maximum Transient Thermal Impedance



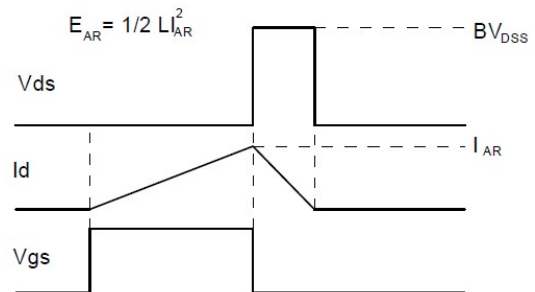
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

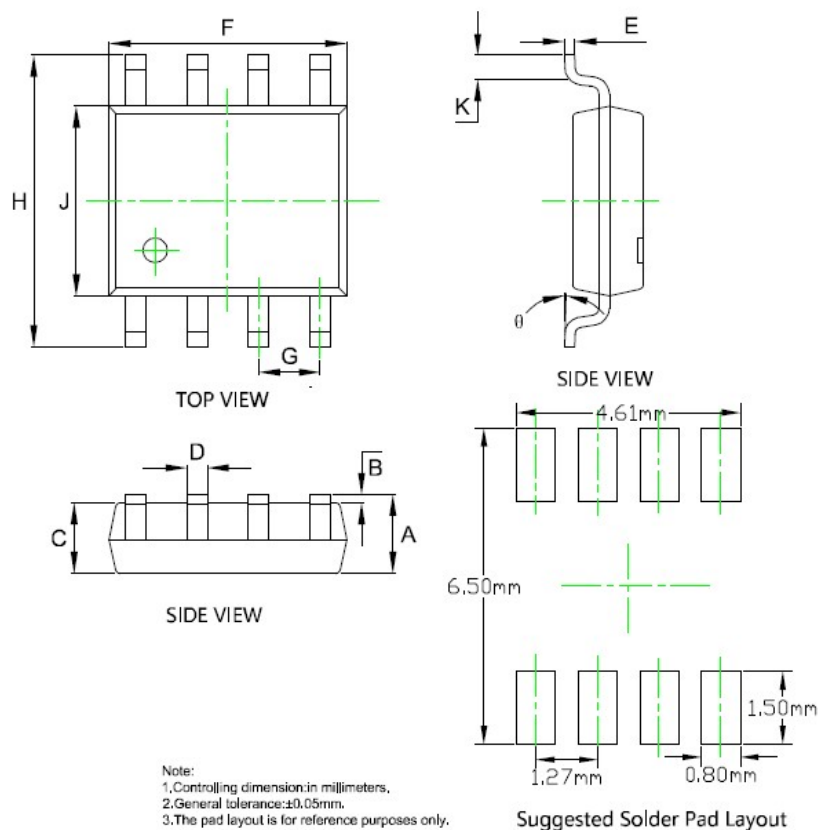


Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

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