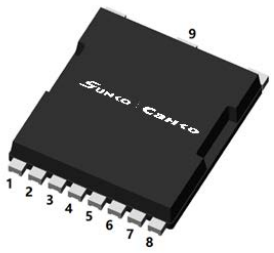
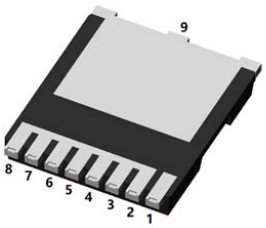
SCT1D4G04AJ

N-Channel Enhancement Mode Field Effect Transistor

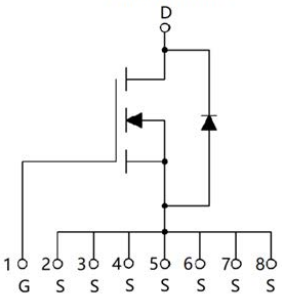


Top View



Bottom View

TOLL



Product Summary

- V_{DS} 40V
- I_D 210A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.4mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜1.9mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	40	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	I_D	32	A
		T_A=100℃		20	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃		210	
		T_C =100℃		132	
Pulsed Drain Current	T_C=25℃, t_p=100μs		I_{DM}	840	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=49A		EAS	600.25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	2.7	W
		T_A=100℃		1.1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		113	
		T_C =100℃		45	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	36	45	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.9	1.1	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCT1D4G04AJ	F1	SCT1D4G04AJ	2000	4000	20000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
		V_{GS}= 0V, I_D=1mA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	-	1	1.4	mΩ
		V_{GS}=4.5V, I_D=25A	-	1.4	1.9	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	3.3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	210	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=1MHz	-	6140	-	pF
Output Capacitance	C_{oss}		-	1860	-	
Reverse Transfer Capacitance	C_{rss}		-	75	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=50A	-	89	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	
Gate-Drain Charge	Q_{gd}		-	15	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A, di/dt=100A/us	-	53	-	nC
Reverse Recovery Time	t_{rr}		-	55	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, I_D=50A R_{GEN}=3Ω	-	14	-	ns
Turn-on Rise Time	t_r		-	15	-	
Turn-off Delay Time	$t_{D(off)}$		-	84	-	
Turn-off fall Time	t_f		-	44	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

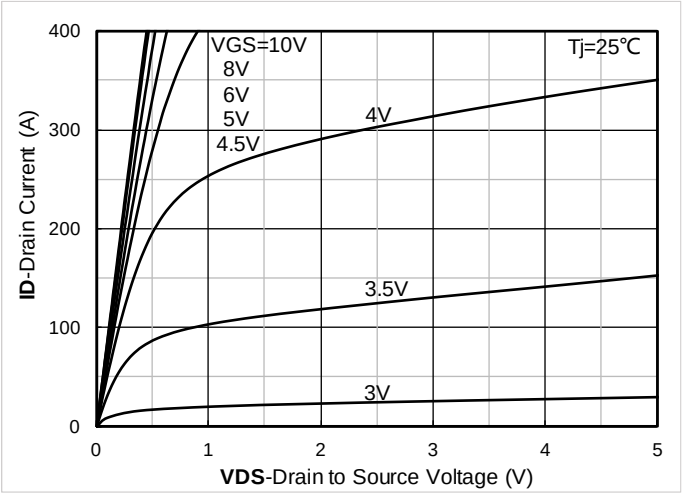


Figure 1. Output Characteristics

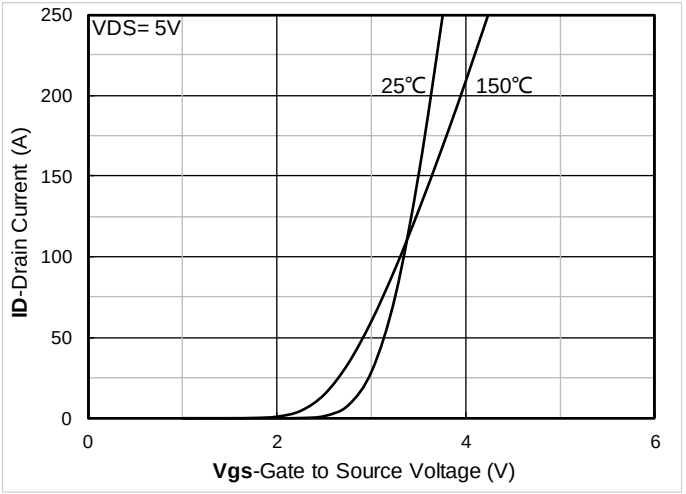


Figure 2. Transfer Characteristics

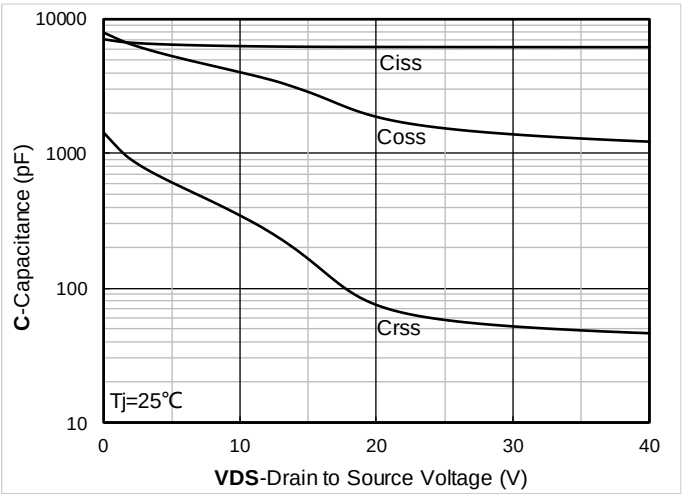


Figure 3. Capacitance Characteristics

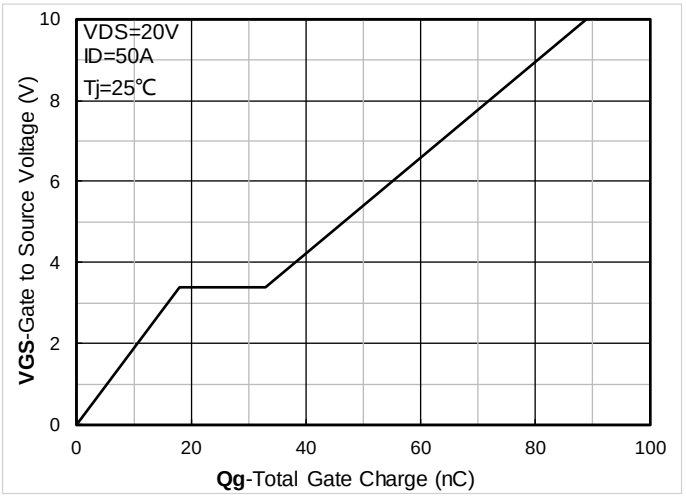


Figure 4. Gate Charge

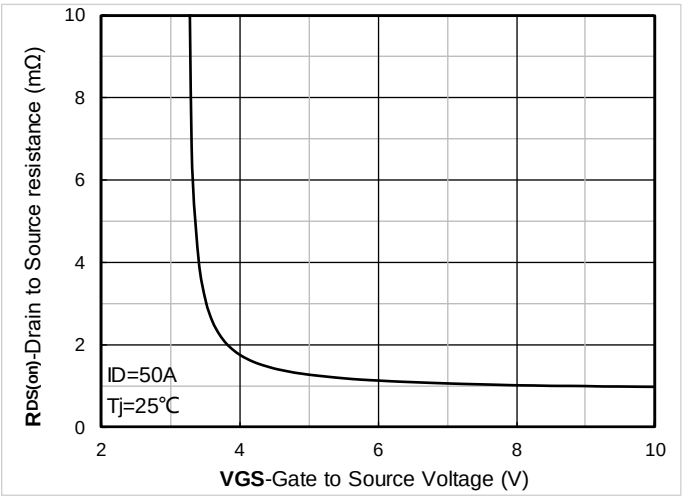


Figure 5. On-Resistance vs Gate to Source Voltage

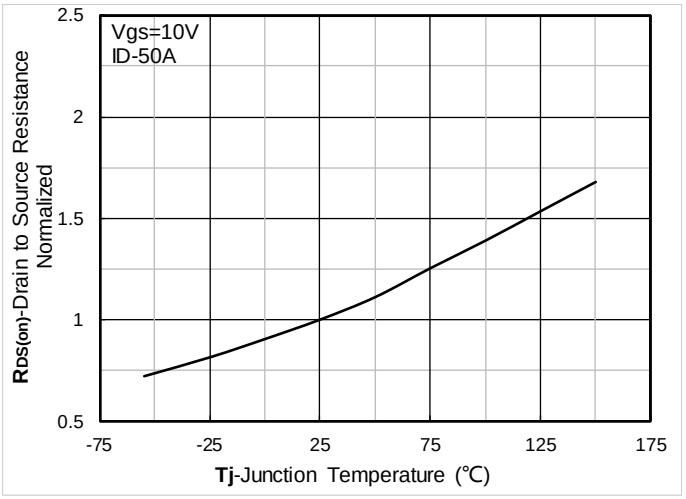


Figure 6. Normalized On-Resistance

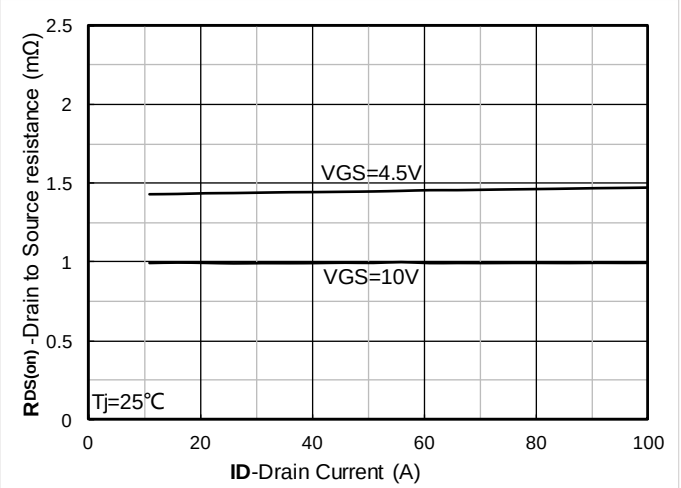


Figure 7. $R_{DS(on)}$ VS Drain Current

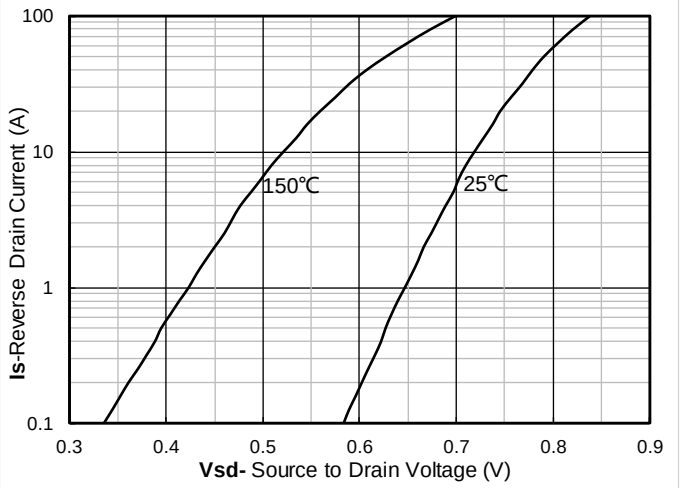


Figure 8. Forward characteristics of reverse diode

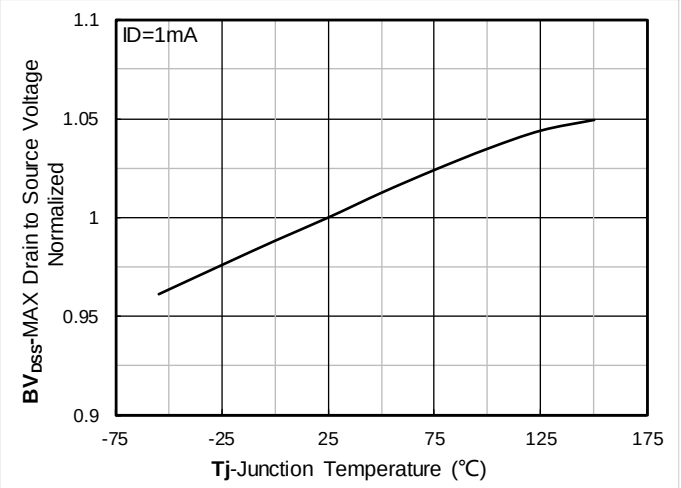


Figure 9. Normalized breakdown voltage

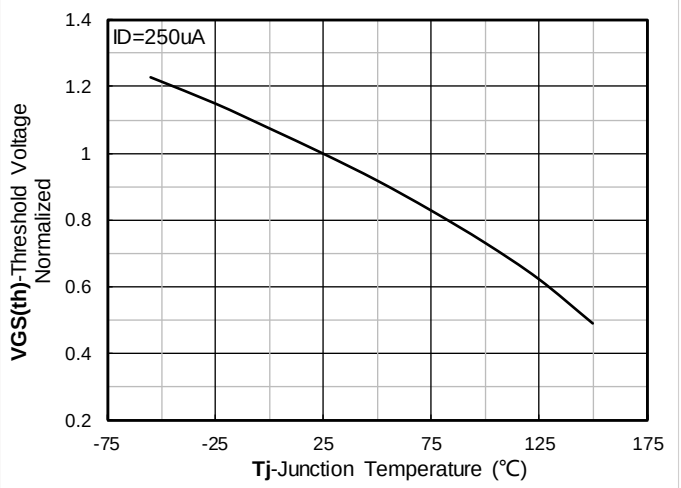


Figure 10. Normalized Threshold voltage

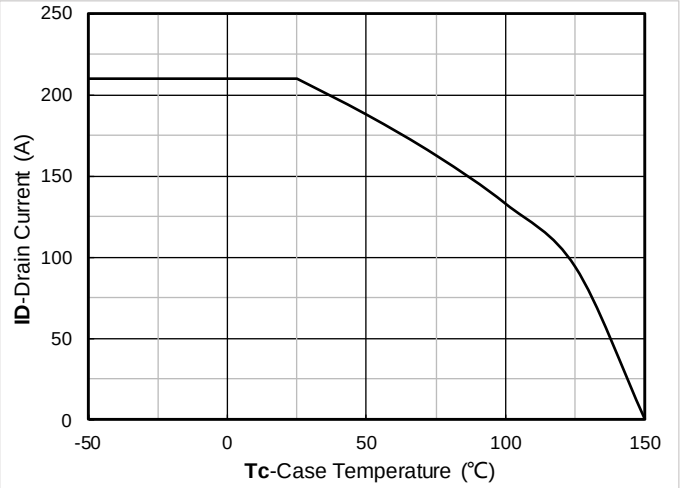


Figure 11. Current dissipation

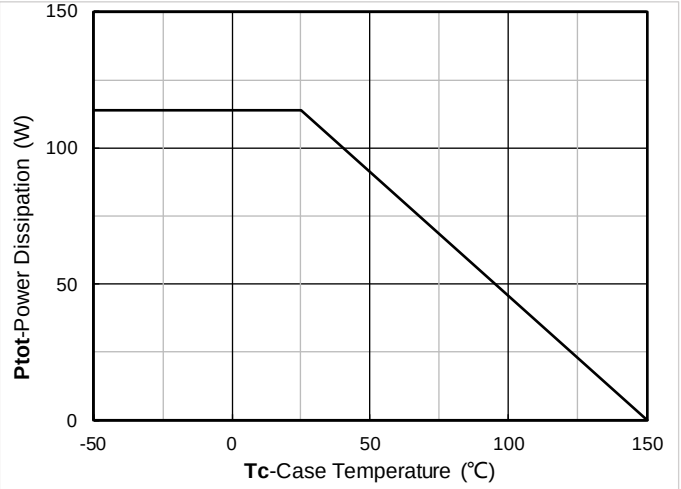


Figure 12. Power dissipation

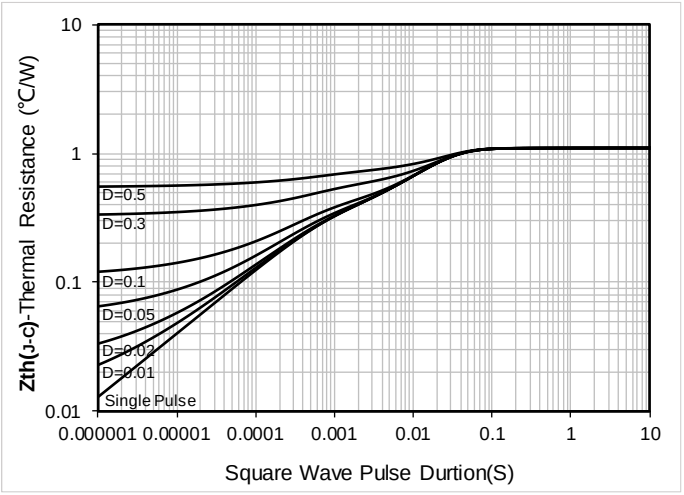


Figure 13. Maximum Transient Thermal Impedance

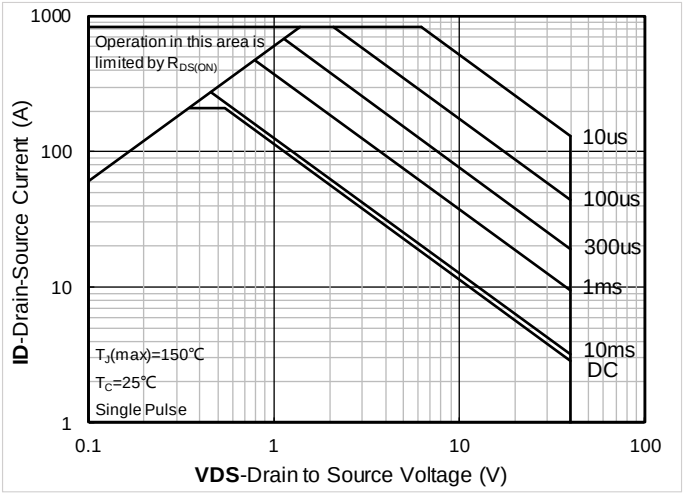


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

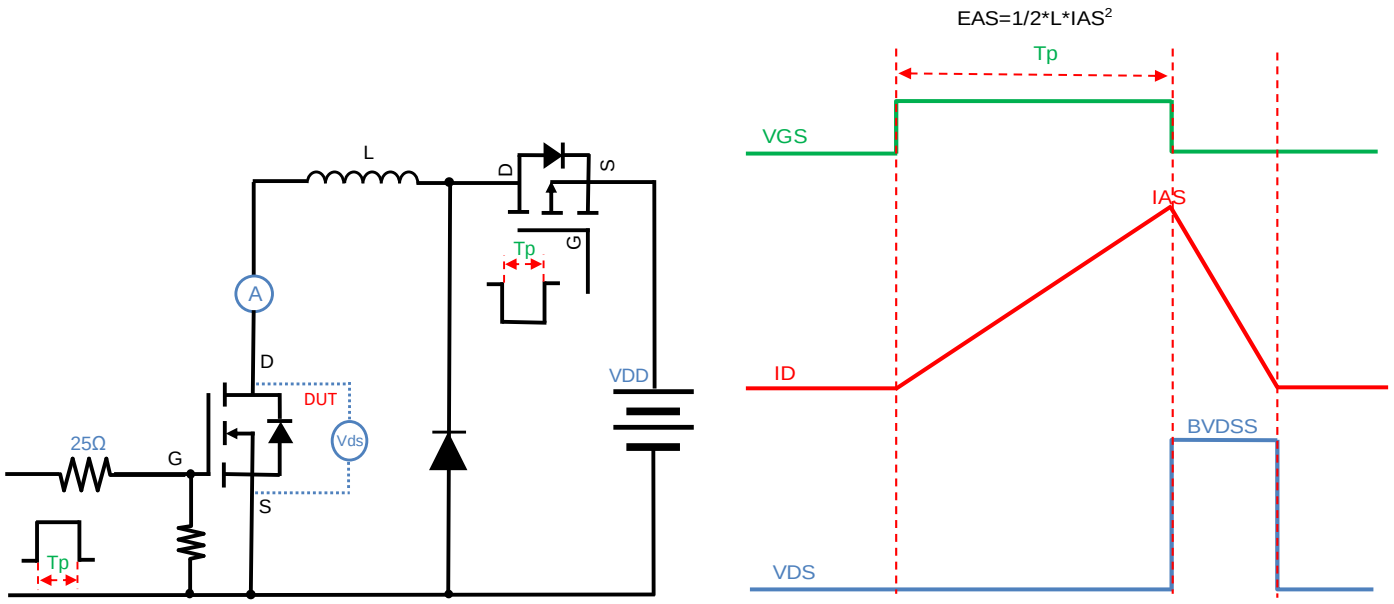


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

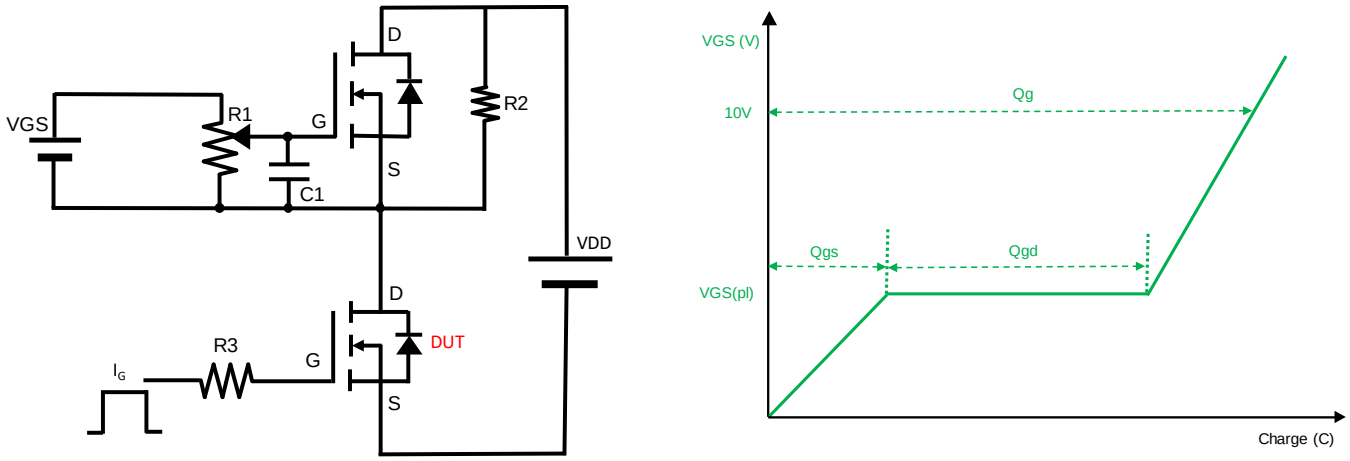


Figure B. Gate Charge Test Circuit & Waveform

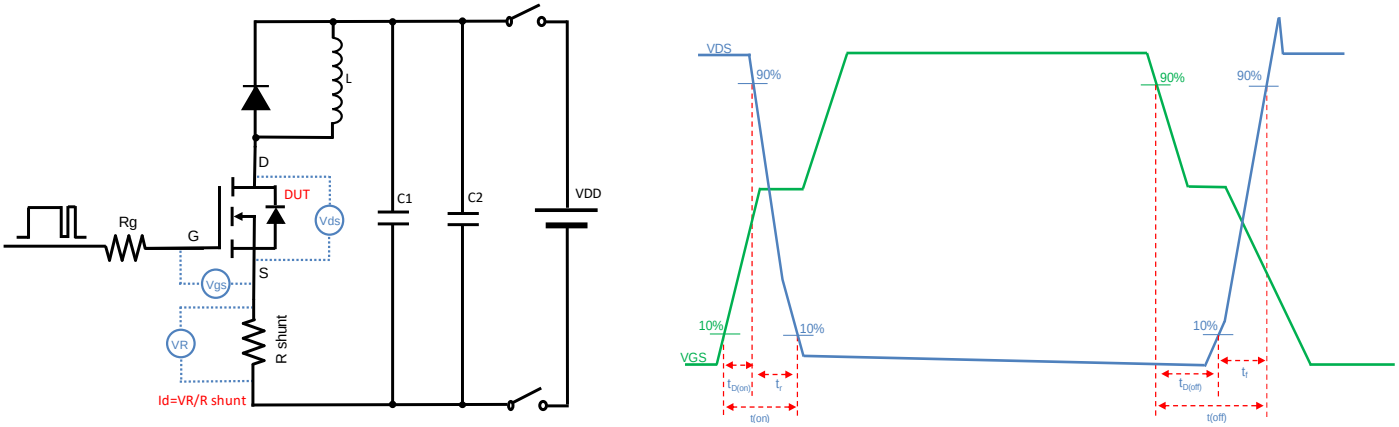


Figure C. Resistive Switching Test Circuit & Waveform

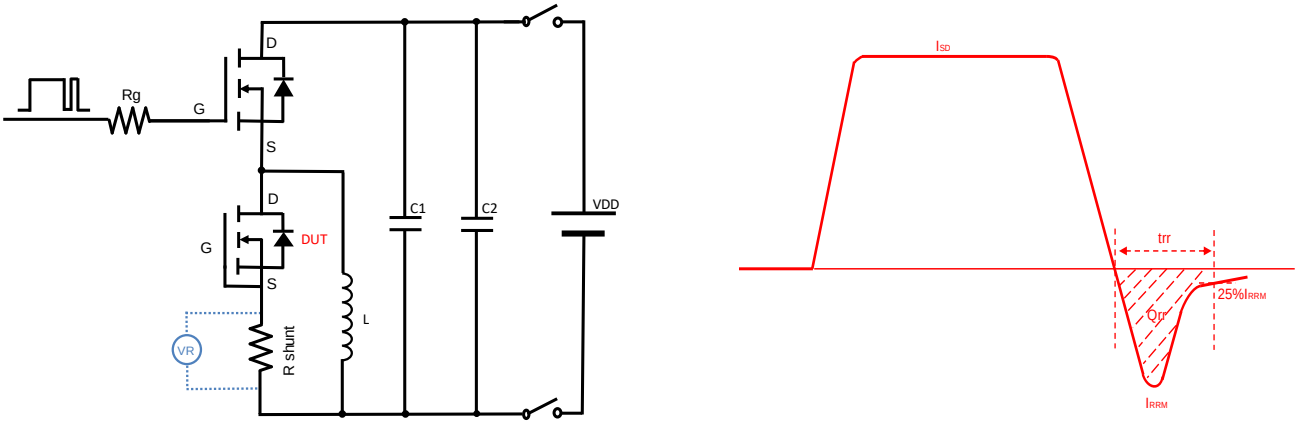
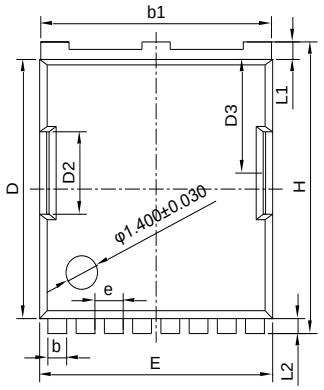
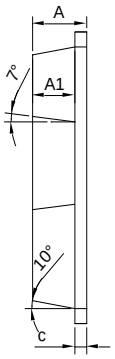


Figure D. Diode Recovery Test Circuit & Waveform

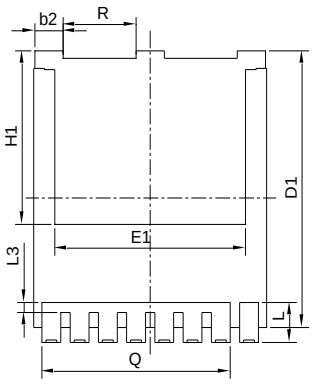
■ TOLL Package information



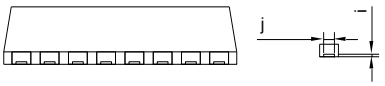
TOP VIEW



SIDE VIEW

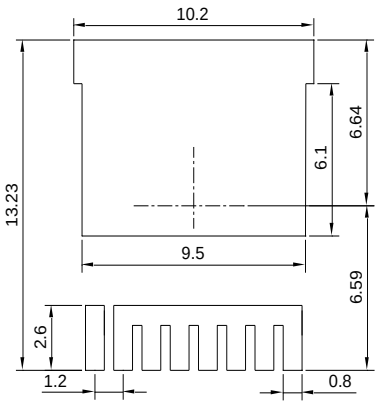


BOTTOM VIEW



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.2	3.3	3.4
D3	4.45	4.55	4.65
E	9.8	9.9	10
E1	8	8.1	8.2
e	1.2 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
i	0.1 REF		
j	0.46 REF		
L	1.5	1.6	1.7
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.3	0.4	0.5
Q	8 REF		
R	3.0	3.1	3.2

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.03mm.
3.The pad layout is for reference purposes only.



SUGGESTED SOLDER PAD LAYOUT
TOP VIEW

UNIT：mm

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