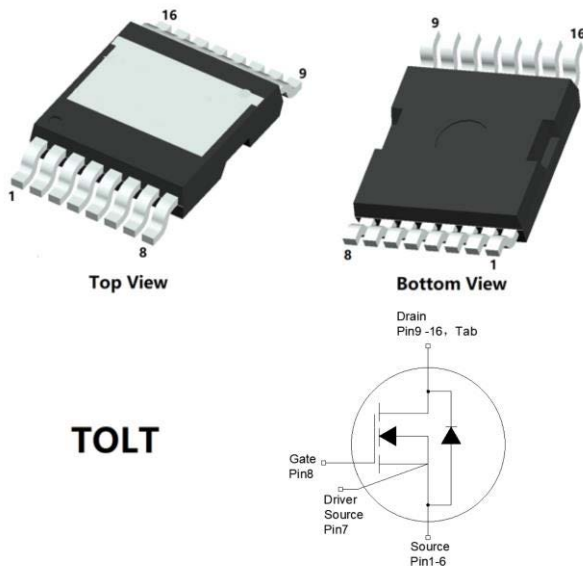


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 340A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<1.7m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High power inverter system
- BMS appliances

■ Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	100	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$	I_D	34	A
		$T_A=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$		24	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$		340	
		$T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$		240	
Pulsed Drain Current	$T_C=25^{\circ}\text{C}$, $t_p=100\mu\text{s}$		I_{DM}	1360	A
Avalanche energy	$V_G=10\text{V}$, $R_G=25\Omega$, $L=5\text{mH}$, $I_{AS}=33\text{A}$		EAS	2722.5	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$	P_D	4.1	W
		$T_A=100^{\circ}\text{C}$		2	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^{\circ}\text{C}$		416	
		$T_C=100^{\circ}\text{C}$		208	
Junction and Storage Temperature Range			T_J , T_{STG}	-55~+175	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	30	36	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.3	0.36	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCTL1D7G10H	F1	SCTL1D7G10H	1200	1200	6000	13" reel

SCTL1D7G10H

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
		V _{GS} = 0V, I _D =10mA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	μA
		V _{DS} =80V, V _{GS} =0 V, T _J =125℃	-	-	100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	2.6	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	1.28	1.7	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.75	1.2	V
Gate resistance	R _G	f=1MHz	-	1.45	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	285	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	10700	-	pF
Output Capacitance	C _{oss}		-	2010	-	
Reverse Transfer Capacitance	C _{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =30A	-	166	-	nC
Gate-Source Charge	Q _{gs}		-	34	-	
Gate-Drain Charge	Q _{gd}		-	49	-	
Reverse Recovery Charge	Q _{rr}	I _F =30A, di/dt=100A/us	-	167	-	nC
Reverse Recovery Time	t _{rr}		-	92	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =30A R _{GEN} =4.5Ω	-	30	-	ns
Turn-on Rise Time	t _r		-	65	-	
Turn-off Delay Time	t _{D(off)}		-	121	-	
Turn-off fall Time	t _f		-	107	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

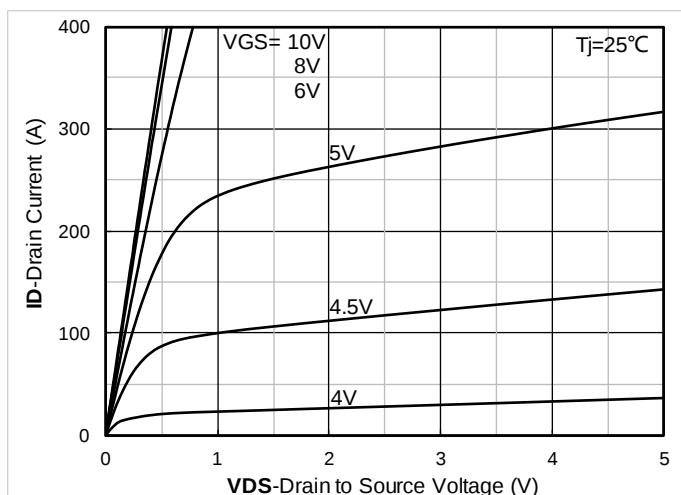


Figure 1. Output Characteristics

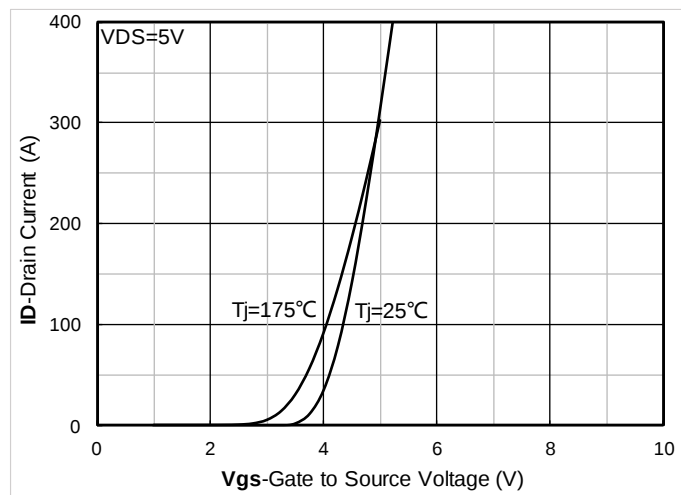


Figure 2. Transfer Characteristics

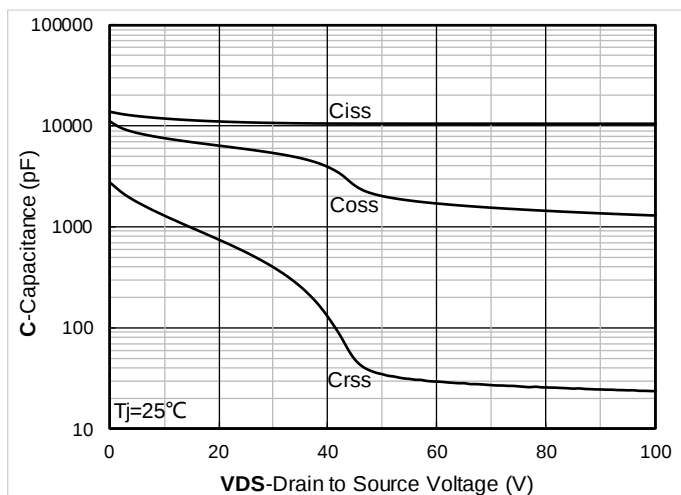


Figure 3. Capacitance Characteristics

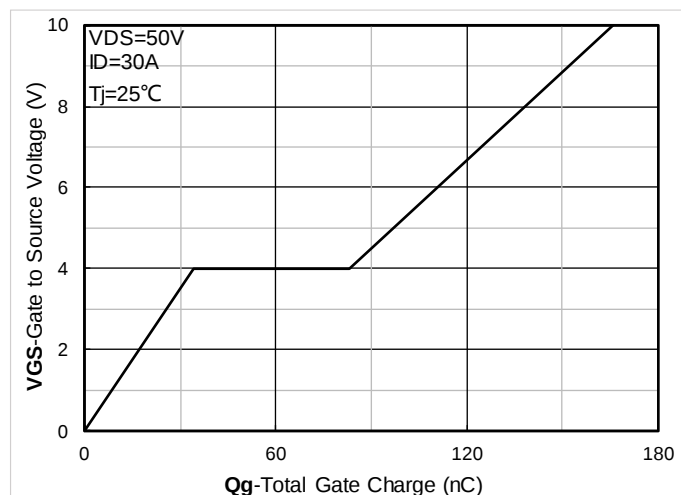


Figure 4. Gate Charge

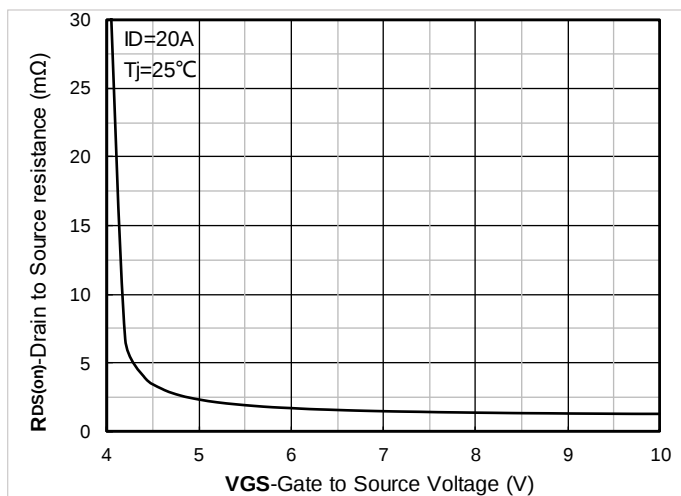


Figure 5. On-Resistance vs Gate to Source Voltage

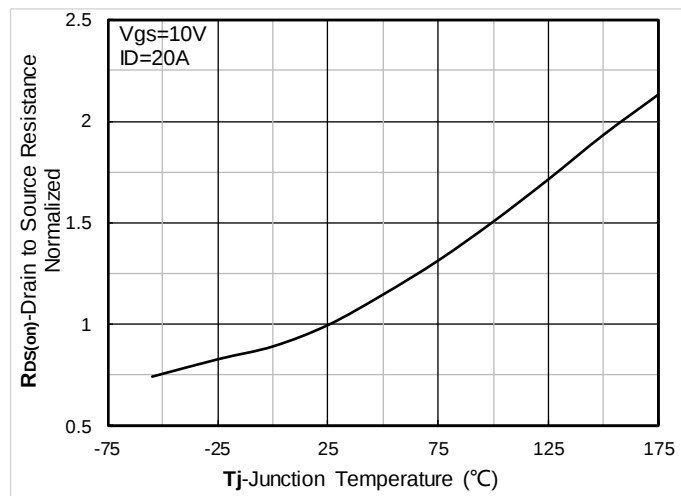


Figure 6. Normalized On-Resistance

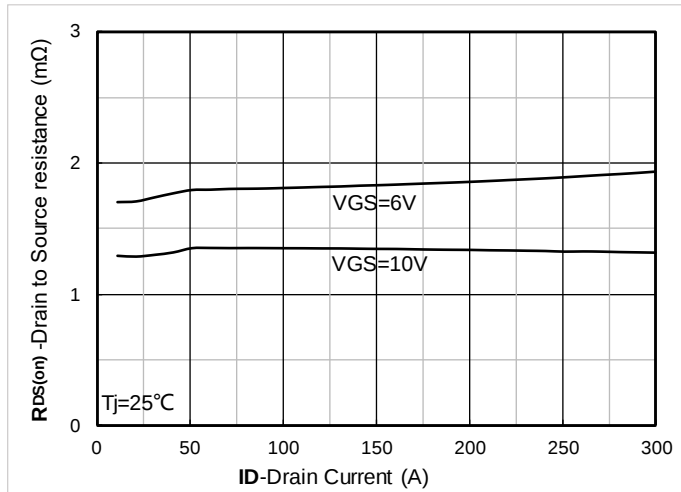


Figure 7. $R_{DS(on)}$ VS Drain Current

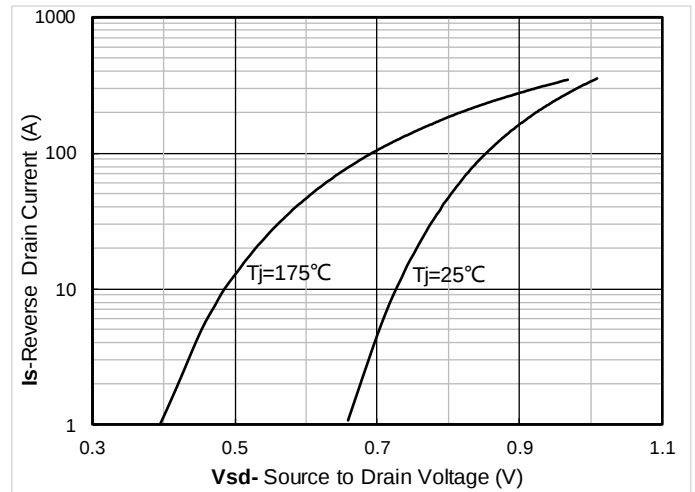


Figure 8. Forward characteristics of reverse diode

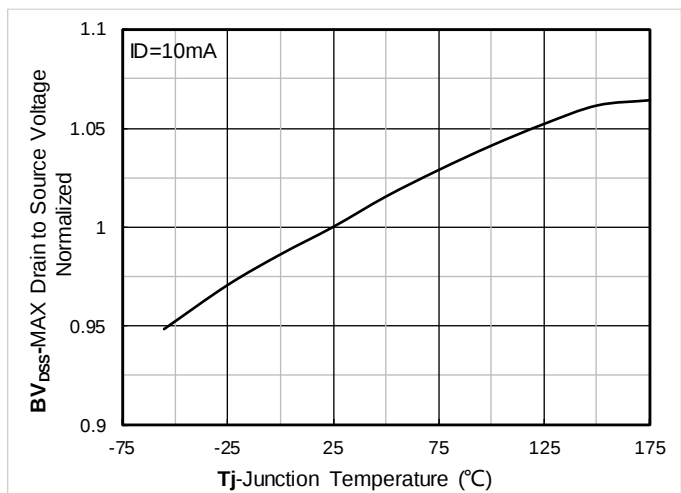


Figure 9. Normalized breakdown voltage

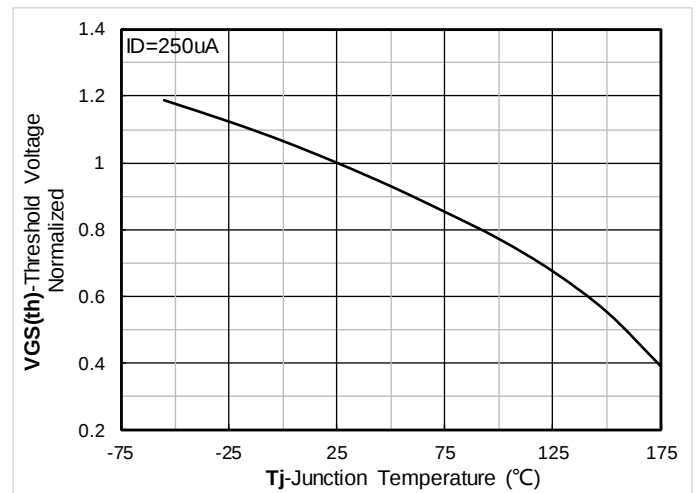


Figure 10. Normalized Threshold voltage

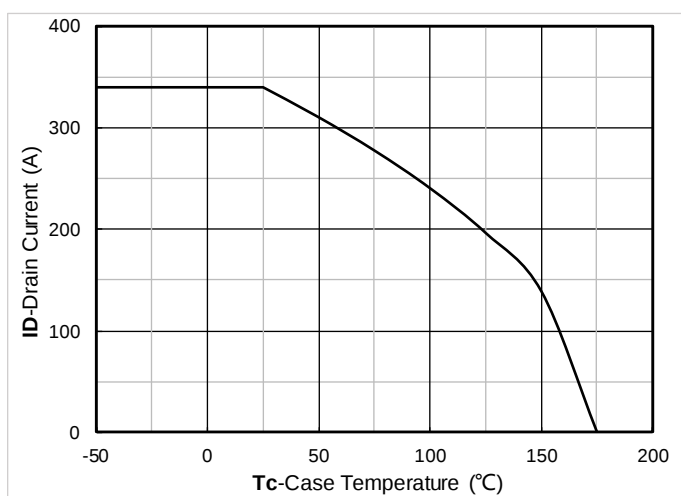


Figure 11. Current dissipation

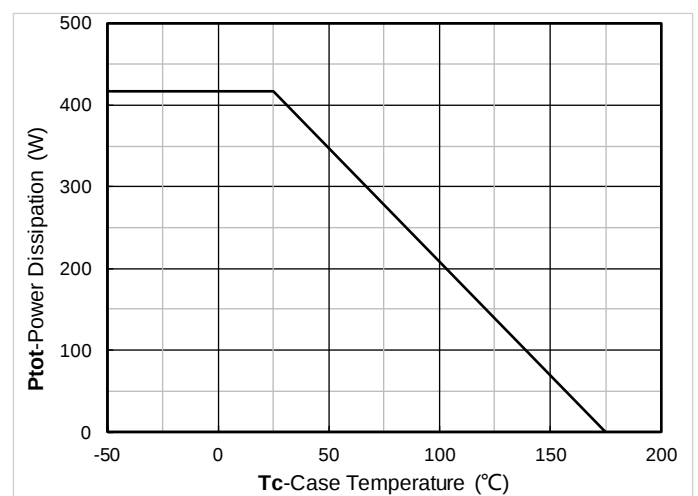


Figure 12. Power dissipation

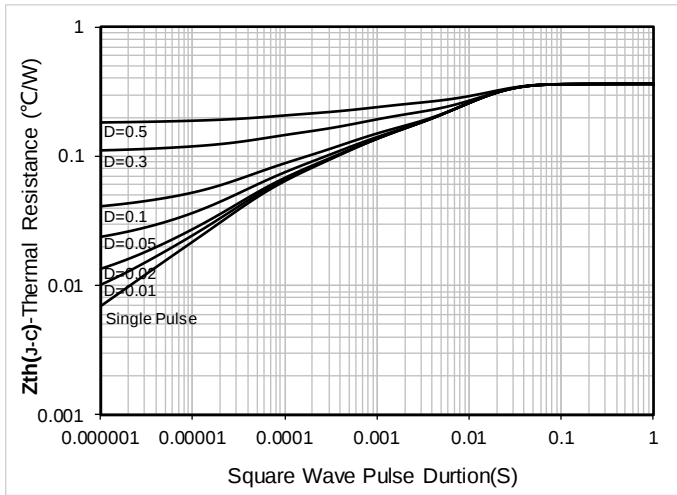


Figure 13. Maximum Transient Thermal Impedance

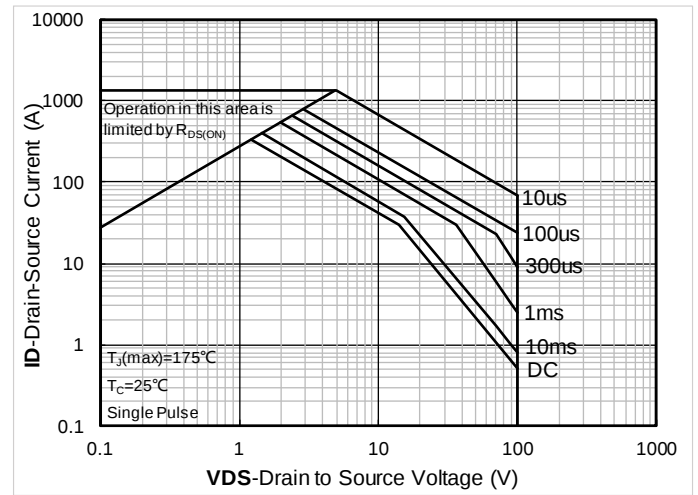


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

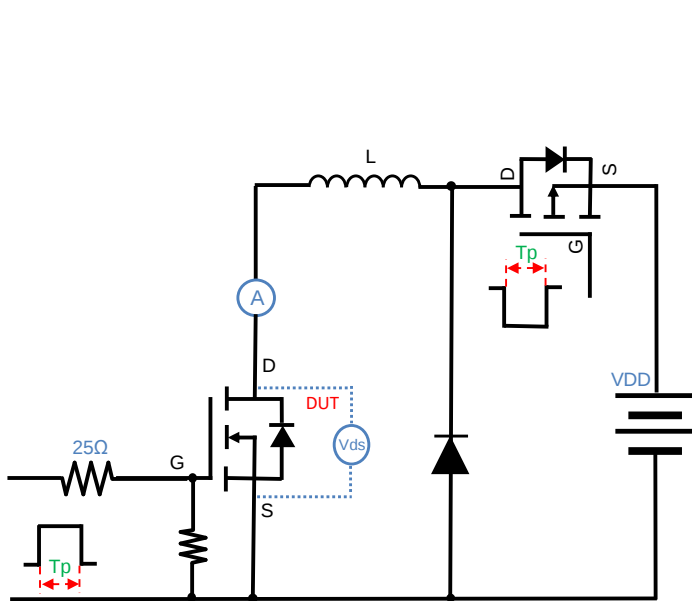
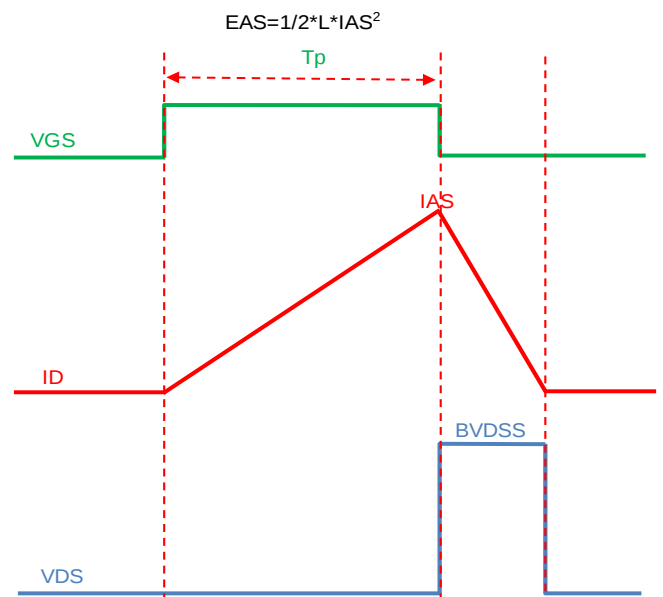


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



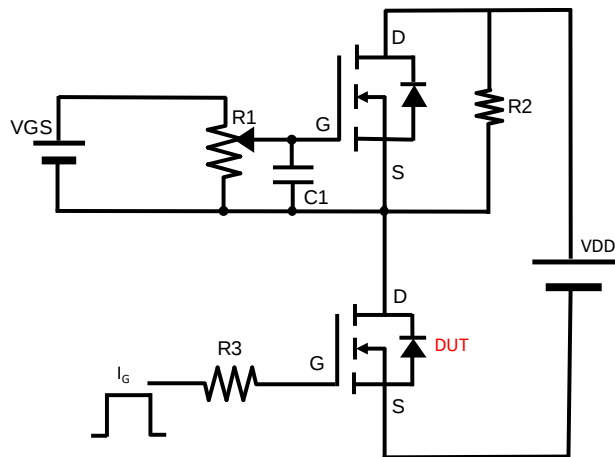


Figure B. Gate Charge Test Circuit & Waveform

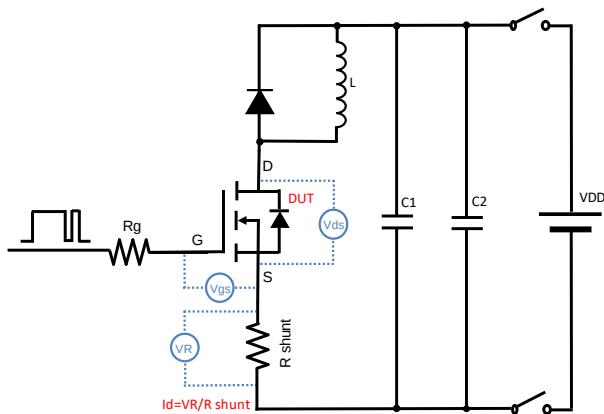


Figure C. Resistive Switching Test Circuit & Waveform

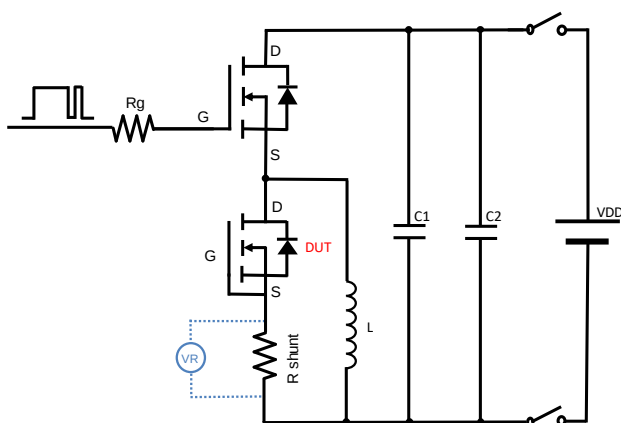
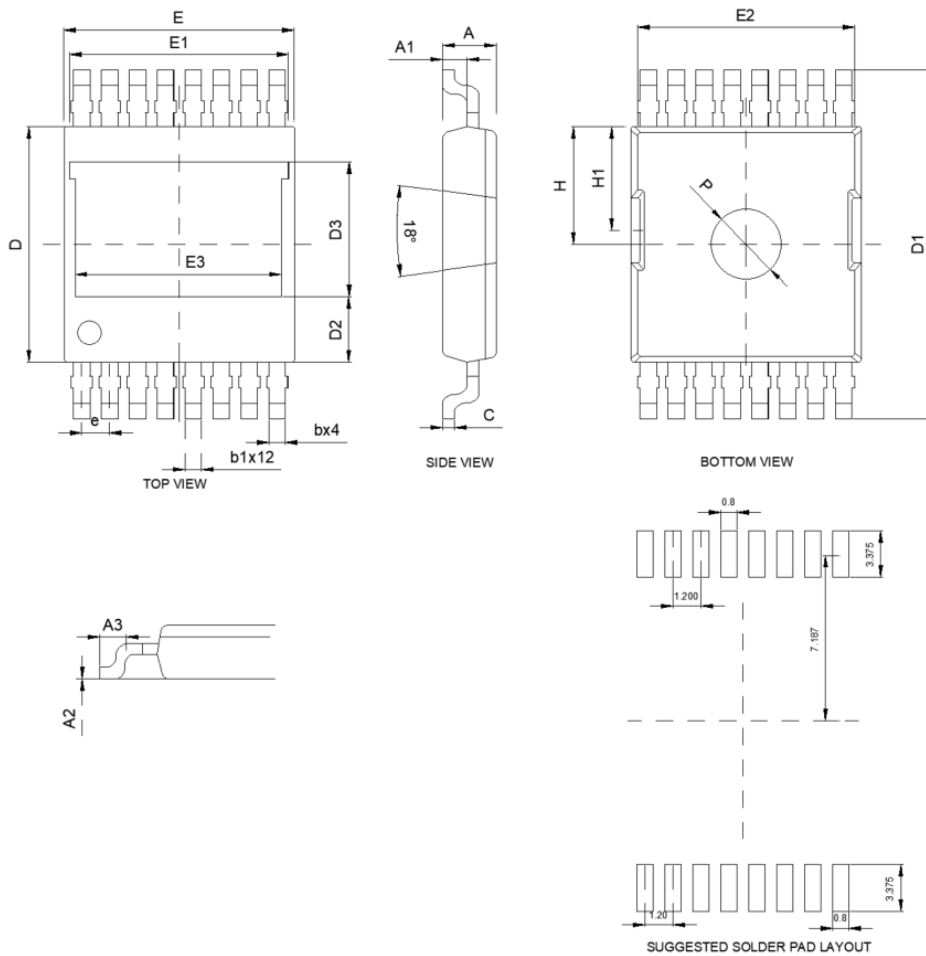


Figure D. Diode Recovery Test Circuit & Waveform

■ TOLT Package information



DIMENSIONS			
SYMBOL	Millimeter		
	MIN	NOM	MAX
A	2.25	2.30	2.35
A1	1.00	1.04	1.08
A2	0.01	0.08	0.16
A3	1.50REF		
b	0.70	0.75	0.80
b1	0.60	0.70	0.80
c	0.40	0.50	0.60
D	10.00	10.10	10.30
D1	14.80	15.00	15.20
D2	2.60	2.80	3.00
D3	5.77REF		
E	9.70	9.90	10.10
E1	9.46REF		
E2	9.25REF		
E3	8.70REF		
e	1.18	1.20	1.22
H	5.00	5.20	5.40
H1	4.40	4.60	4.80
L	2.40	2.45	2.50
P	2.80	3.00	3.20

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY

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