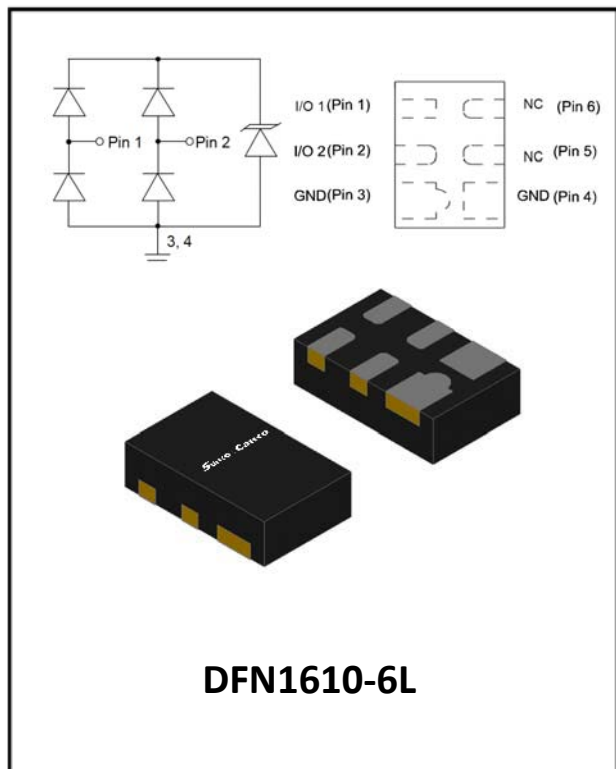


2-Line, Uni-directional, Ultra-low Capacitance Transient Voltage Suppressor



Features

- Stand-off voltage: 5V Max
- Transient protection for each line according to IEC61000-4-2(ESD): $\pm 20\text{kV}$ (contact)
IEC61000-4-5(surge): 5A (8/20 μs)
- Low leakage current
- Low clamping voltage
- Compliant

Applications

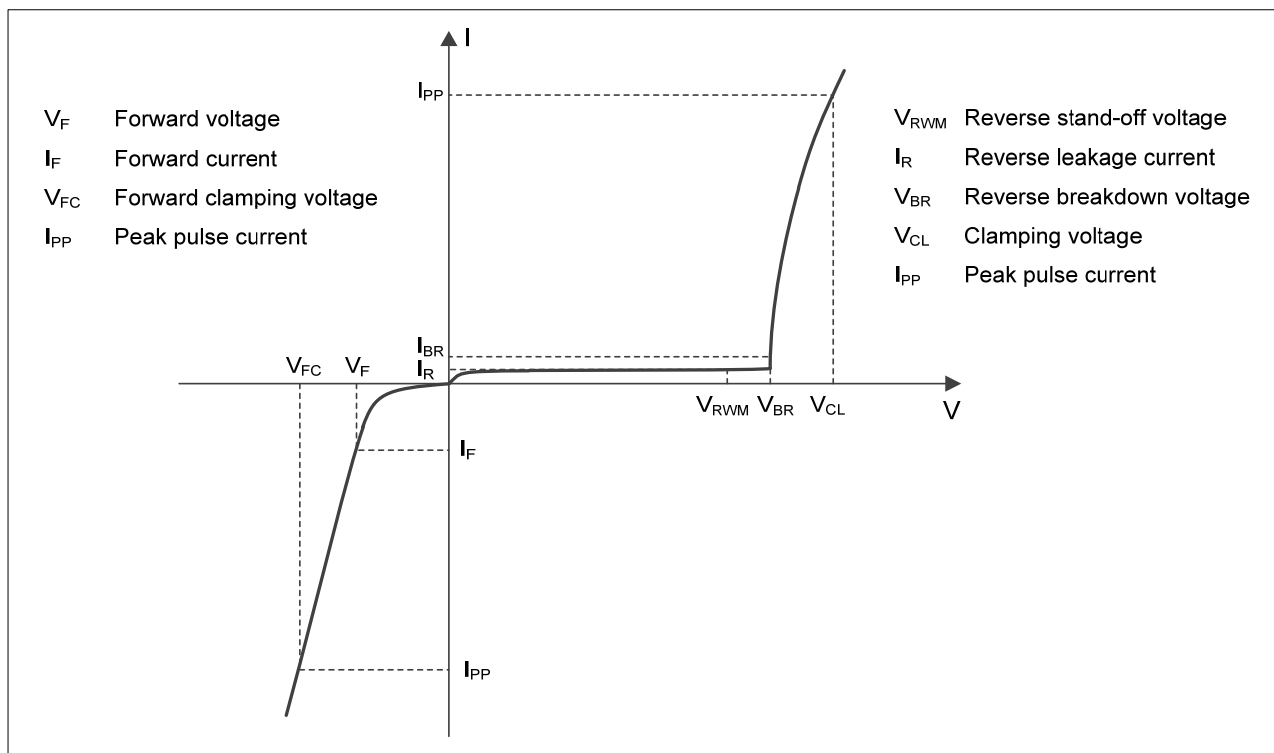
- Cellular Handsets and Accessories
- USB Ports
- Video Interface
- MDDI Ports

Mechanical Data

- Package: DFN1610-6L
- Case Material: "Green" Molding Compound
- Moisture Sensitivity: Level 3 per J-STD-020
- Marking Information: See Below



■Definitions of electrical characteristics



■Maximum Ratings

PARAMETER	SYMBOL	LIMITS	UNIT
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	60	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 25	kV
ESD according to IEC61000-4-2 contact discharge		± 20	
Junction temperature	T_J	-55~125	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

■Electrical Characteristics ($T_a=25^{\circ}C$ Unless otherwise specified)

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V_{RWM}	V				5
Reverse leakage current	I_R	μA	$V_{RWM} = 5V$			0.6
Reverse breakdown voltage	V_{BR}	V	$I_T = 1mA$	6		
Clamping voltage ¹⁾	V_{CL}	V	$I_{PP} = 1A, t_p = 8/20\mu s$ any I/O pin to ground			9
		V	$I_{PP} = 5A, t_p = 8/20\mu s$ any I/O pin to ground			12
Junction capacitance	C_J	pF	$V_R = 0V, f = 1MHz$ any I/O pin to ground		0.5	0.8
Junction capacitance	C_J	pF	$V_R = 0V, f = 1MHz$ between I/O pins		0.3	0.4

Notes:

(1). Non-repetitive current pulse, according to IEC61000-4-5.

■Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(mg)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
ESDSL0502P6	F1	Approximate 2.5	3 000	30 000	120 000	7" reel

■ Characteristics (Typical)

Fig.1 8/20 μ s waveform per IEC61000-4-5

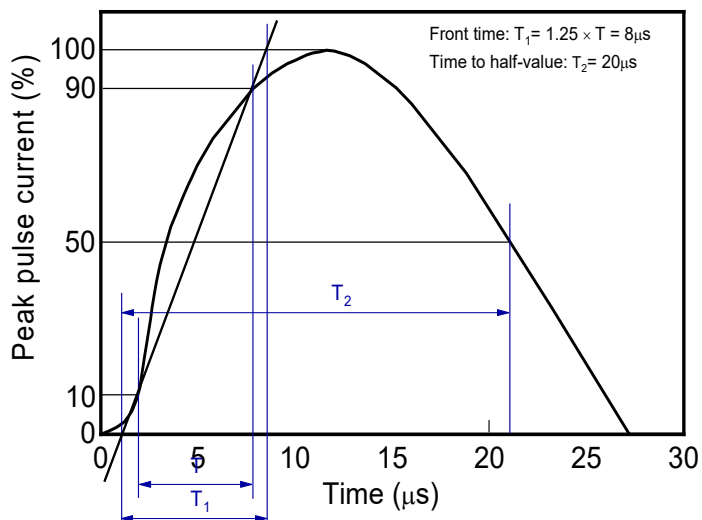


Fig.2 Contact discharge current waveform per IEC61000-4-2

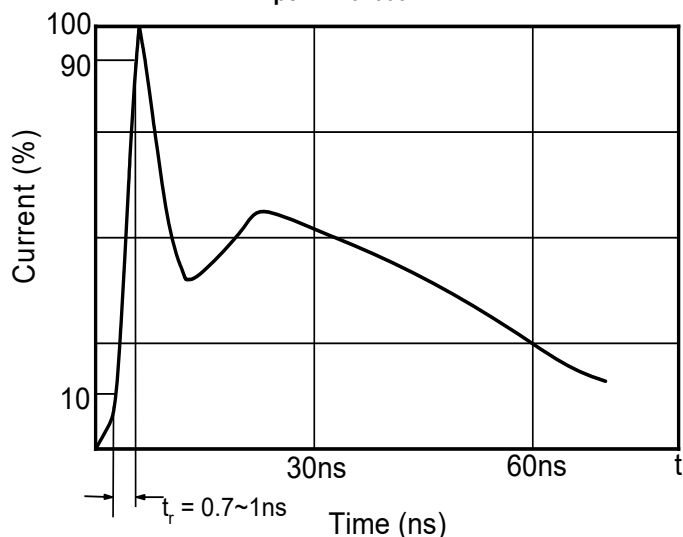


Fig.3 Clamping voltage vs. Peak pulse current

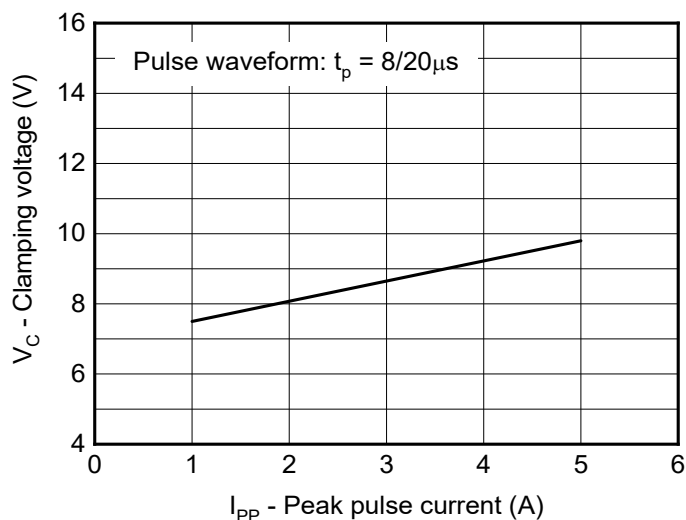


Fig.4 Capacitance vs. Reverse voltage

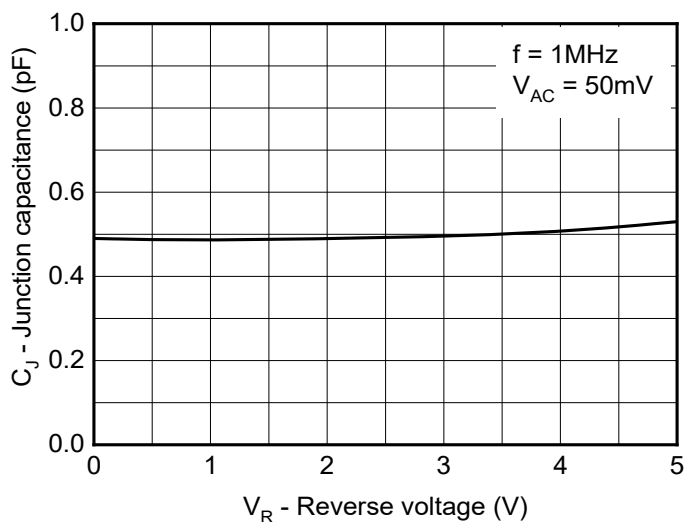


Fig.5 Non-repetitive peak pulse power vs. Pulse time

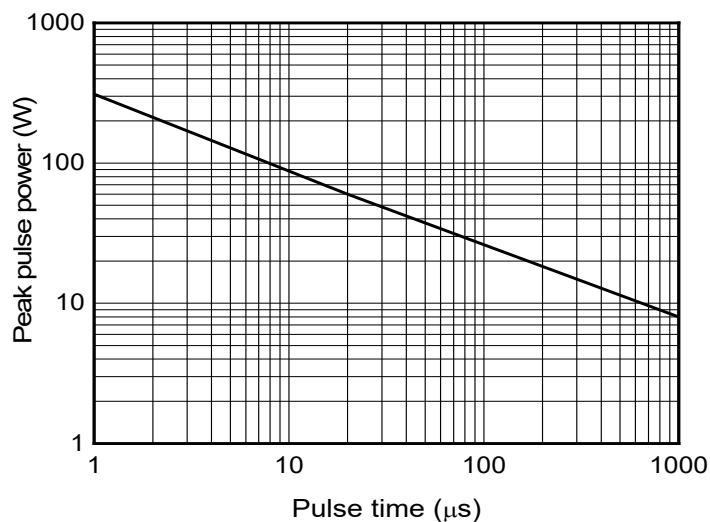


Fig.6 Power derating vs. Ambient temperature

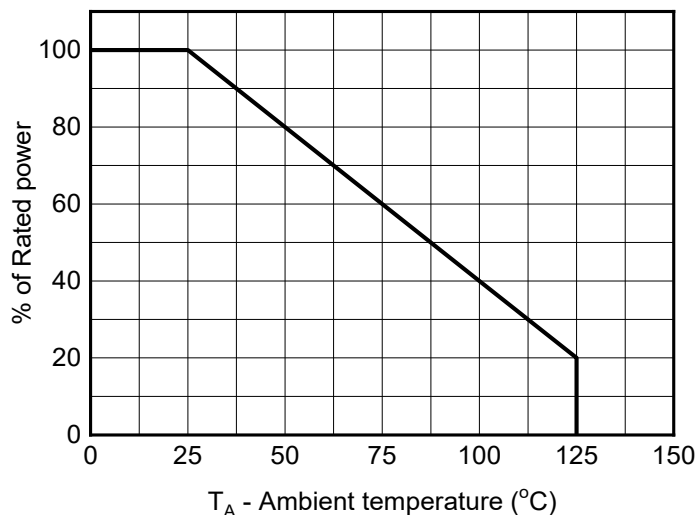


Fig.7 ESD clamping
(+8kV contact discharge per IEC61000-4-2)

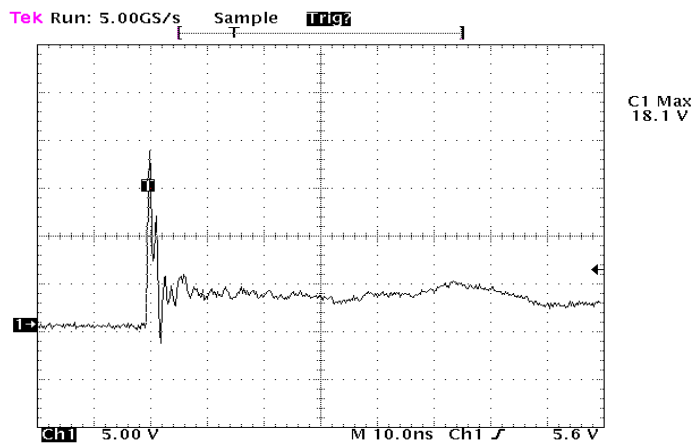
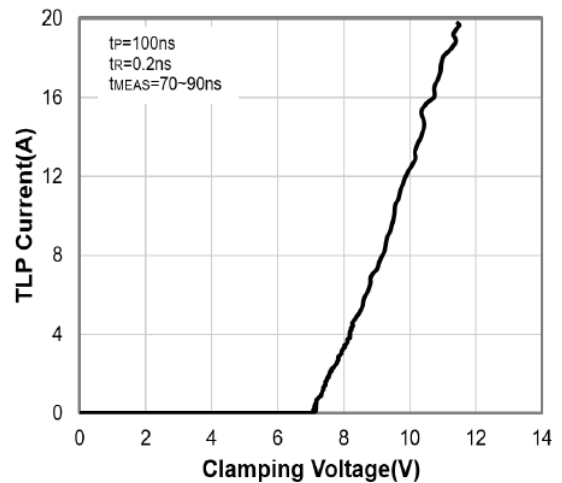
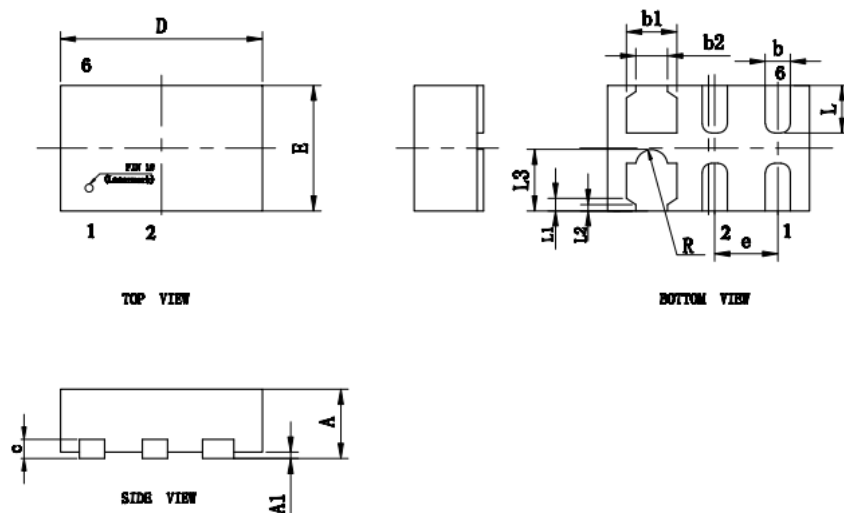


Fig.7 TLP Measurement

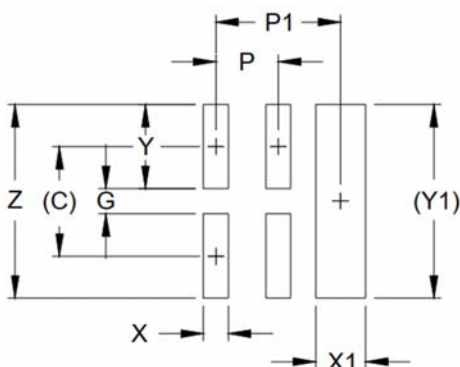


Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	-	0.02	0.05
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
b2	0.20	0.25	0.30
c	0.10	0.15	0.20
D	1.55	1.60	1.65
E	0.95	1.00	1.05
e	0.50 BSC		
L	0.33	0.38	0.43
L1	0.100REF		
L2	0.05REF		
L3	0.49REF		
e	0.08	0.13	0.18

Recommended PCB Layout



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.87)
G	.007	0.19
P	.020	0.50
P1	.039	1.00
X	.008	0.20
X1	.016	0.40
Y	.027	0.68
Y1	(.061)	(1.55)
Z	.061	1.55

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met

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