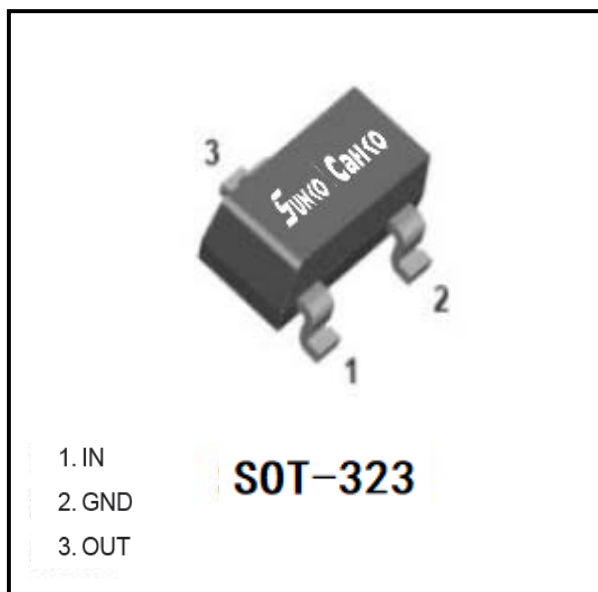


Digital Transistors (Built-in Resistors)



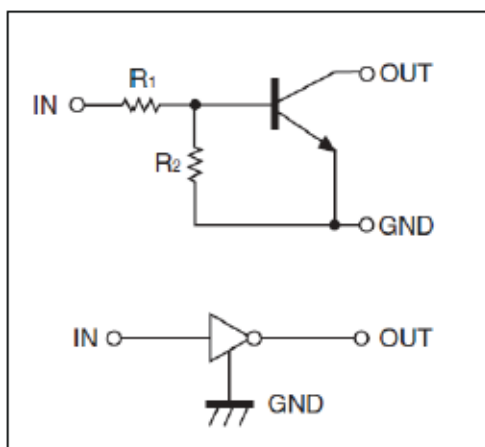
Features

- Epoxy meets UL-94 V-0 flammability rating
- Moisture Sensitivity Level 1
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion
- NPN

Mechanical Data

- **Package:** SOT-323
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** 43

■Equivalent circuit



■Maximum Ratings (Ta=25°C Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Supply Voltage	VCC	V		50
Input Voltage	VIN	V		-7 to +20
Output Current	IO	mA		100
Power Dissipation	PD	mW		200
Junction Temperature	Tj	°C		150
Storage Temperature	TSTG	°C		-55 to +150

DTC143XUA

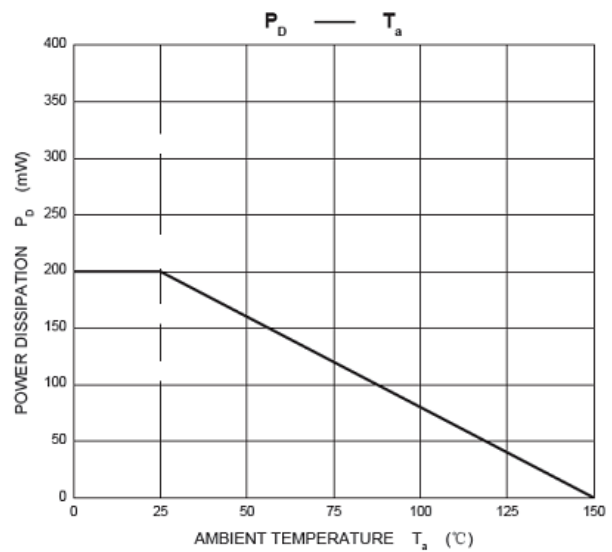
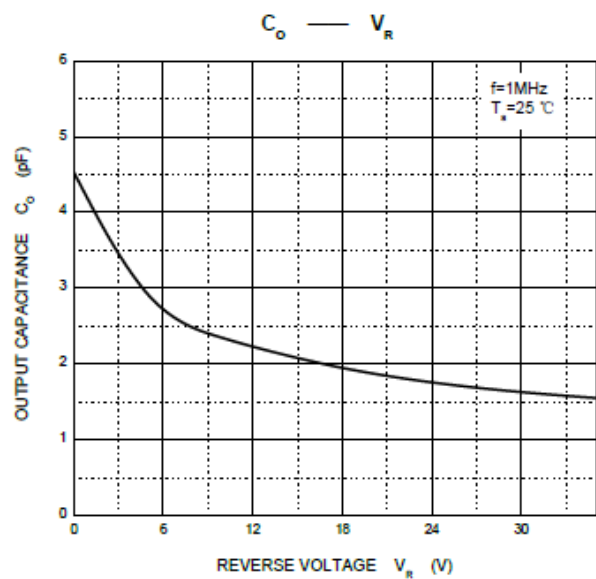
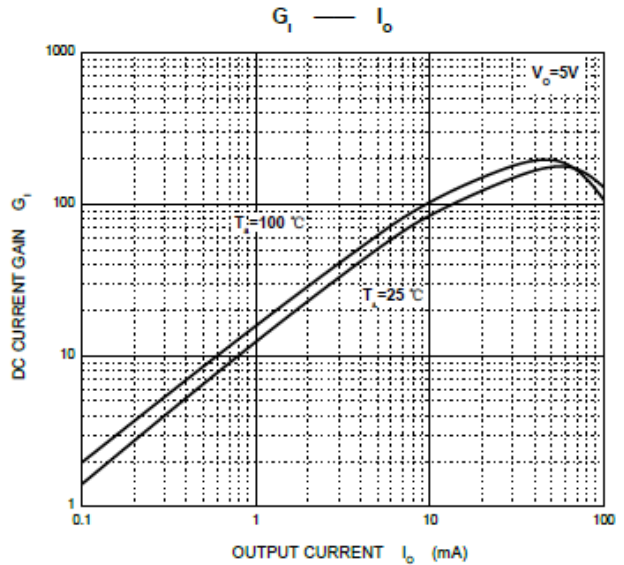
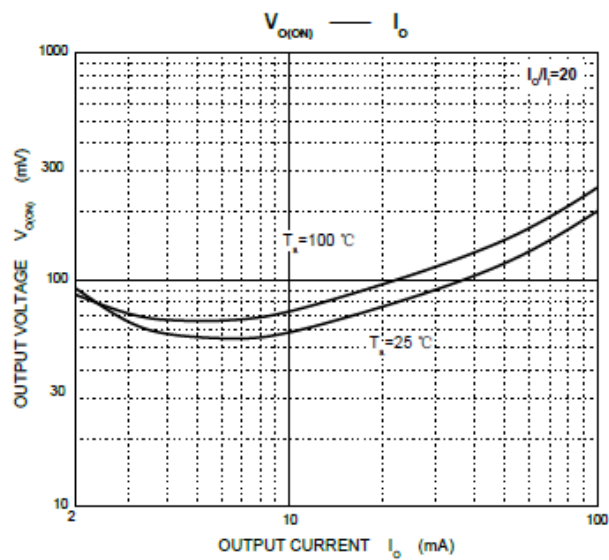
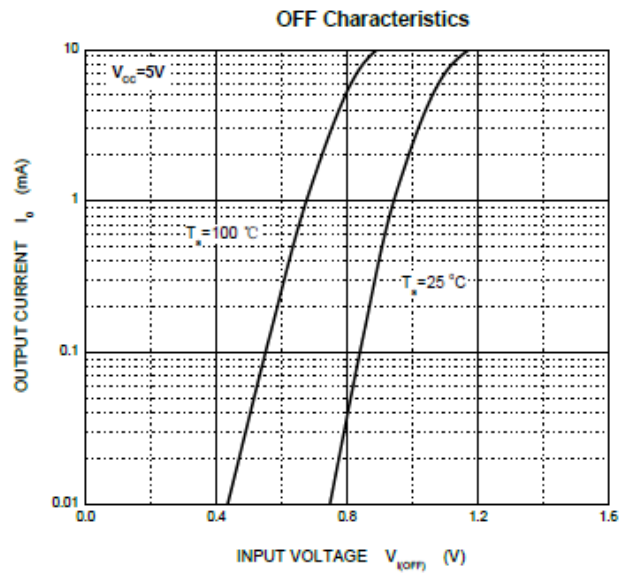
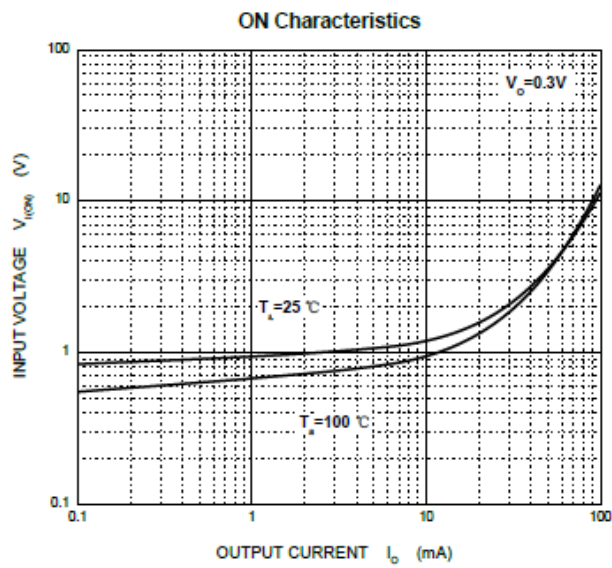
■ Electrical Characteristics (Ta=25°C unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	$V_{I(off)}$	V	$V_{CC}=5V, I_c=100\mu A$ $V_o=0.3V, I_c=20mA$	0.3		
	$V_{I(on)}$	V				2.5
Output voltage	$V_{O(on)}$	V	$I_o / I_i = 10mA / 0.5 mA$			0.3
Output current	$I_{O(off)}$	μA	$V_{CC}=50V, V_i=0$			0.5
DC current gain	GI		$V_o=5V, I_o=10mA$	30		
Input resistance	R_1	$k\Omega$		3.29	4.7	6.11
Resistance ratio	R_2/R_1			1.7	2.1	2.6
Transition frequency	fT	MHz	$V_o=10V, I_o=5mA, f=100MHz$		250	

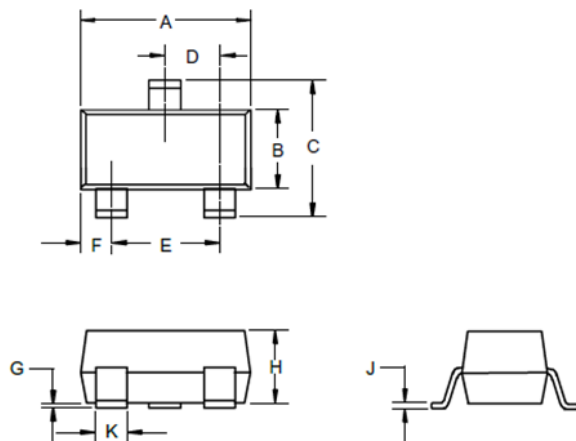
■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTC143XUA	F2	Approximate 0.005	3000	30000	120000	7" reel

■ Characteristics (Typical)

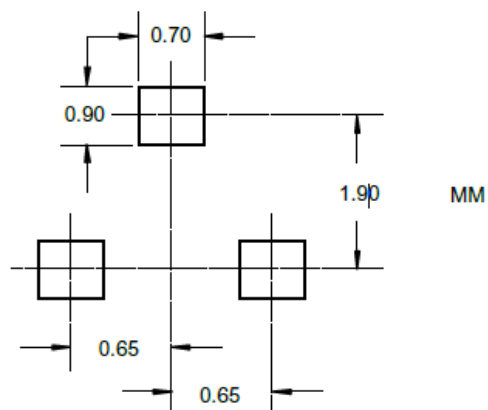


■ SOT-323 Package Outline Dimensions



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.071	.087	1.80	2.20	
B	.045	.053	1.15	1.35	
C	.083	.096	2.10	2.45	
D	.026 Nominal		0.65Nominal		
E	.047	.055	1.20	1.40	
F	.012	.016	.30	.40	
G	.000	.004	.000	.100	
H	.035	.039	.90	1.00	
J	.004	.010	.100	.250	
K	.006	.016	.15	.40	

■ SOT-323 Suggested Pad Layout



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